Performance Evaluation of an 11-Level Multilevel Inverter with Reduced Power Switch Configuration

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Abstract

This thesis aims to construct and explore a symmetrical (10S-11L) and asymmetrical (12S-15L) multilevel inverter based on the structural analysis of a suggested system with a decreased switching parameter. By adding the necessary number of power switches, this suggested architecture may be implemented at the N-Level. The suggested multilevel inverter model is developed utilizing normalized switching technique and multicarrier PWM technology in comparison to well-known MLI topologies. The Normalized Switching method and Driving training based optimization (DTBO) are used to find the switching angles for this topology. In order to reduce the THD level in compliance with IEEE 519.2014 rules, the suggested topology was further studied using the Multicarrier Alternative Phase Opposition Disposition (APOD) PWM approach. The suggested system was put through a number of test scenarios, including ones with various modulation indices, various DC input voltages, various loads, and voltage ride-through capabilities. This thesis includes a variety of simulation and experimental findings that demonstrate how the suggested multilevel inverter topology functions in various configurations.

1.INTRODUCTION

Nabae introduced the concept of multilayer inverters (MLIs) for the first time in 1980, and those working in the field of inverter innovation paid close attention to it. For medium- and high-power applications, Nabae is interested in constructing innovative topologies for multilevel inverters that employ lower-power switches, as well as creating novel topologies for higher power demanding applications. MLIs are engaged in a variation of industries due to their advantageous characteristics, and their use can

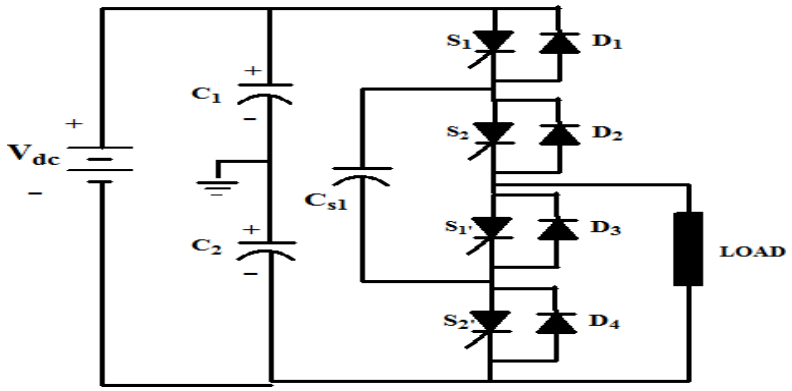
be observed in a number of fields, including Fuel Cell (Jain et al. 2015), STATCOM (Deniz et al. 2007), FACTS (Sotoodeh & Miller 2013), Static Synchronous Series Compensator (SSSS) (Geethalakshmi & Dananjayan 2009), Direct Torque Control based induction motor. Switching losses, device strains, the need for more clamping diodes, and problems with voltage balancing capacitors may all be reduced thanks to MLI. A multilevel output is often created by connecting and controlling various voltage levels related with several DC voltage sources that are wired in succession with one another.Based on how many DC voltage sources they employ, MLIs have been separated into two groups: those with a single DC voltage source and those with multiple DC voltage sources. The type of MLIs with just a single DC power supply are the most common. To construct DC/AC conversion systems that require little and medium power, flying capacitor inverters (FCI) and diode clamping inverters (DCI), which are industry standards, are frequently employed. Multi-DC voltage sources are inverters that employ multiple DC voltage sources, such as a cascaded inverter. These inverters are used for high-power operations like dynamic voltage restorers, static VAR correction, and grid inverters for environmentally friendly energy conversion systems. Simply put, diode clamped and flying capacitors are less efficient than cascaded inverters. Modified H-bridge inverters (MHBI) and cascaded H-bridge inverters (CHBI) are the often utilized forms of cascaded inverters.. The electromagnetic compatibility, lower switching losses, decreased voltage strains between power switches, decreased total harmonic distortion (THD), and decreased dv/dt stresses in applications involving sustainable power sources make the cascaded H-Bridge inverter the most promising alternative MLI. Cascaded H-Bridge Inverters (CHBI) are categorized as each symmetrical or asymmetrical liable on the magnitude of the DC source voltage. The DC voltage bases used in the symmetrical arrangement are equal. however, in the asymmetrical arrangement, they are different (Nanda et al. 2019, Sotoodeh & Miller 2013). CHB also faces a variety of difficulties. It requires the usage of many DC sources when used in a continuous power transition framework, which raises the price of the inverter as a result. The application of balanced symmetrical and asymmetrical design has recently enabled the realization of a significant number of

novel topologies. With a minimum of circuitry, these combinations are utilized to study various topologies.

Several resounding topologies for power quality applications are currently being researched, including the Filled U-cell (PUC) topology (Ounejjar et al. 2015, Rajesh et al. 2018), Modular Multilevel Converter (MMC) topology (Sotoodeh & Miller 2013), Modified T-type topology (Hosseinzadeh et al. 2018), Cross Switched Topology (Kamaldeep & Kumar 2016), Two topologies that employ asymmetric arrangement to create their circuits are filled U-cell (PUC) and hybrid.The multiple & Sinusoidal pulse width modulation , which utilize three or more levels (Gupta et al. 2020), are two examples of modulation techniques that the multilevel inverter can use depending on the inverter architecture. Building a method of modulation that can be smeared to a variety of unlike applications is important for it to be efficient. The vast majority of real-time inverters in use today employ sine pulse width modulation technology since it is so prevalent. Multi-pulse width modulation (MPWM), harmonic injection pulse width modulation, space vector pulse width modulation, choosy harmonic removal pulse width modulation, and hysteresis-controlled PWM are just a few of the options available to designers and manufacturers. Level-shifted pulse width modulation techniques and phase-shifted PWM techniques are the two different forms of pulse width modulation (PWM) approaches for multi-carrier systems (McGrath & Holmes 2002).Three primary categories of level removed PWM: alternative phase opposition disposition (APOD), phase disposition (PD), and phase opposition disposition (POD). Level shifting is the most often used, but also most difficult, technology in single-phase cascaded inverter systems. Selective harmonic elimination (SHE) PWM and space vector PWM (Grigoletto 2021) are two more modulation techniques that have drawn a lot of attention. The research center is focusing on creating new tools and machinery for handling harmonics, which will be used in alternating current drive systems and electrical systems at the transmission and distribution levels.

Inverter with Multilevel Capacitor Clapping

The Multilevel Inverter's clamped capacitance is sometimes referred to as a flying capacitor clamped because it relies on the device potential to one capacitance voltage range and the device voltages to a different capacitor voltage level. When S1 and S1' are turned on, the clamping capacitor C1 is charged; conversely, when S2 and S2' are turned on, it is discharged. A schematic of the three level capacitance clamped circuit is presented in Figure 1. Table 1 displays component analyses in relation to the total amount of levels (L).Multilevel inverters of the sort known as flying capacitor multilevel inverters are created with reduced distortion for high energy as well as higher power uses. Flying capacitors, which are utilized to fasten the voltage that flows across the power semiconductor components, are employed in this system. A distribution static compensator (DSTATCOM) is made using this MLI, and it is evaluated using the hysteresis current regulation approach to regulate the current that the DSTATCOM injects (Shukla et al. 2007).



(Source: Fang Lin Luo 2017)

Figure 1.Three-level Clamped Capacitor MLI

Table 1. Capacitor Clamped MLI component analysis based on level (L)

Parameters	Formulation based on Levels (L)
IGBTs / MOSFETs	2*(L-1)
Capacitors with DC linkage	0.5*L *(L-1)
Switching Diodes	(L-1)
Total components	(L-1)*(0.5L+3)
DC link capacitor voltage	V_{dc} / (L-1)

(Devesh Raj *et al.* 2022)

Zhang et al. (2020) present a switched-capacitor based active-capacitor-clamped inverter with 7 stages of operation for usage in electric vehicle (EV) applications. It is made up of a diode, seven transistors, a self-balancing voltage regulators, a bidirectional switch, and three capacitors. This inverter may be able to use just one alternating current source to produce a 1.5 voltage gain. Because all power switches' greatest blocking voltages do not surpass the dc input voltage, they are all under minimal voltage stress. All of the voltage ripples brought on by capacitors during POD-PWM modulation are carefully analyzed.

SYMMETRICAL N-LEVEL MULTILEVEL INVERTER

The hierarchical design discussed in this chapter is for an N-level, single-phase, balanced H-bridge multilevel structure with less power automatic switches, as shown in Figure. 2. The switches at T1, T2, T3, T4, and Th1 are unidirectional switches in this setup. The switches Ta, Tb, and Tm have two directions. As inputs, DC voltage sources V1, V2, V3,..., and Vn are used. Ten power semiconductor control switches will be needed for the envisaged eleven-level MLI. For the nine-level MLI, nine power semiconductor control switches are needed.

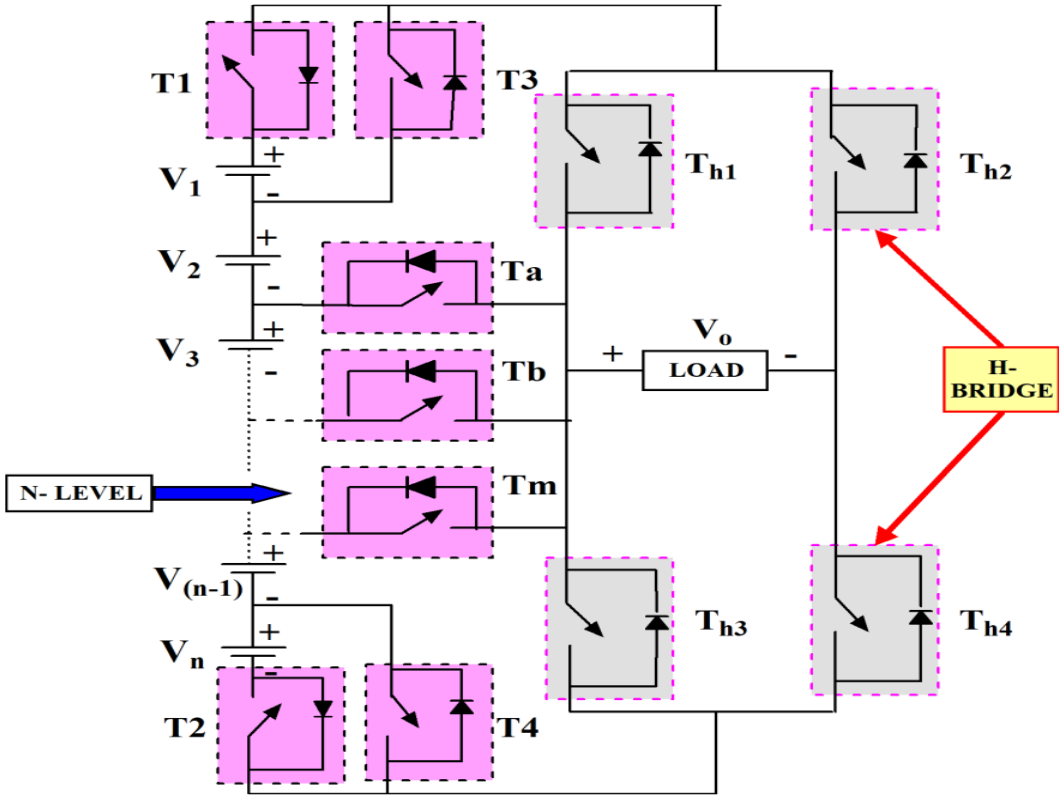


Figure 2. Suggested N-level MLI topology configuration

Addition of one switch for each raised level, which helps in moving this topology for N-level applications. This topology may be used with a wide range of inverters. As shown in the following Equation (1), the necessary for bidirectional switches ranges from zero to seven level configurations. The quantity needed for bidirectional switches (m) corresponds to the sum of levels (L).

$$m = 0, \qquad L \leq 7$$

$$m = \frac{L-7}{2}, \qquad L \geq 9 \tag{1}$$

The suggested single-phase symmetrical 'N' level MLI architecture's DC sources, electrical elements, switches, gate driver request, and total standing voltage are all connected to the number of levels (L) and are each described by Equations (2) to (5), respectively.

$$DC\ Source\ Required = \frac{(N-1)}{2} \quad (2)$$

$$Power\ Electronics\ Switches\ Required = \frac{(N+9)}{2} \quad (3)$$

$$Gate\ Driver\ Circuits = \frac{(N+9)}{2} \quad (4)$$

$$Total\ Standing\ Voltage = 2\ (N+1)Vdc \quad (5)$$

where the input DC voltage sources' amplitudes are indicated by the letters V1, V2, V3,..., Vn. Four DC sources are needed to power the inverter's nine levels as well as its nine active main switches for creating the first level of topology 9S-9L MLI. There are a total of five separate DC sources needed to provide the ten active main switches that the 10S-11L MLI controls with the eleven distinct level output waveforms. In directive to build a fifteen-level output waveform with twelve primary switches for 12S-15L MLI, seven separate DC sources are mandatory. The number of switching devices required is lower than with other topologies since only one switch is required for each higher level. As a result, the THD is given a lot of attention as we progress to higher levels of topology. The 10S-11L topology that has been presented may operate in both symmetrical and asymmetrical formats. As a result, for every additional level that is nine or above, the number of power semiconductor control switches is raised by one. As a consequence, the suggested inverter has fewer components, which lowers the cost of the inverter and simplifies the regulator of the inverter. The implementation of various levels and its switching needs are covered in Table 1.

Operating Principles of Proposed 10S-11L MLI

In order to achieve the required level in MLI, a number of switch from T1 to T10 must be switched ON and OFF for a specific amount of time, as shown in Table 1. Figure 3 displays an eleven-level waveform, 5 DC sources with comparable voltage magnitudes, 8 unidirectional power semiconductor switches, 2 bidirectional power semiconductor switches, and five power electronic sources. The recommended inverter

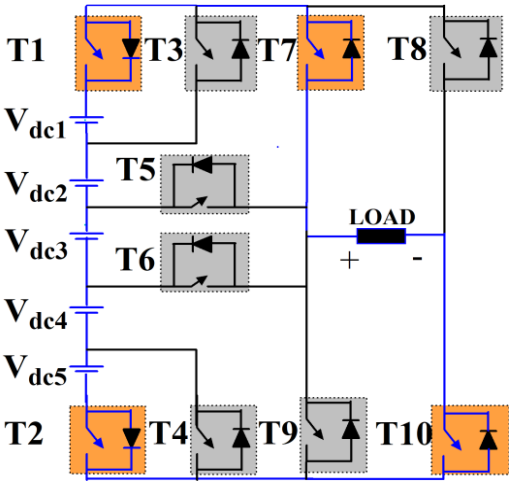
has an H-bridge that is surrounded by 4 unidirectional switches (T7, T8, T9, and T10). Turning on T7 and T10 generates positive voltage, whereas turning on T8 and T9 generates negative voltage. T5 and T6 are both bidirectional modifications. The switches T1, T2, T3, and T4 are all unidirectional. Table 3.2 displays the recommended multilayer inverter's shifting table for generating different voltage levels. According to Mode 1 in Figure 4(a), the input voltage (Vdc1+ Vdc2+ Vdc3+ Vdc4+ Vdc5 = +5Vdc) are linked to the load's voltage through switches T1, T2, T7, and T10. According to Mode 2 in Figure 4(b), the source of voltage (Vdc2+ Vdc3+ Vdc4+ Vdc5 = +4Vdc) is delivered to the load through T2, T3, T7, and T10.

Table 2 Switching table for 10S-11L MLI level generation

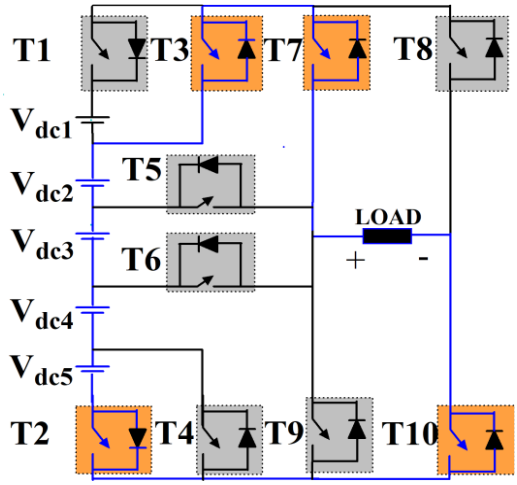
Mode	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	Output
1	1	1	0	0	0	0	1	0	0	1	+5
2	0	1	1	0	0	0	1	0	0	1	+4
3	0	1	0	0	1	0	0	0	0	1	+3
4	0	1	0	0	0	1	0	0	0	1	+2
5	0	0	0	1	0	1	0	0	0	1	+1
6	0	0	0	0	0	0	1	1	0	0	0
7	0	0	0	0	0	0	0	0	1	1	0
8	0	0	1	0	1	0	0	1	0	0	-1
9	1	0	0	0	1	0	0	1	0	0	-2
10	1	0	0	0	0	1	0	1	0	0	-3
11	1	0	0	1	0	0	0	1	1	0	-4
12	1	1	0	0	0	0	0	1	1	0	-5

The input voltage (Vdc3+ Vdc4+ Vdc5 = +3Vdc) is applied to the load through T2, T5, T7, and T10 in accordance with Mode 3 of Figure 3(c). Figure 3 (d) displays how T2, T6, T7, and T10 connect the load to the source voltage (Vdc4+Vdc5 = +2Vdc). T4, T6, T7, and T10 are used to link the input voltage (Vdc5 = + Vdc) to the load producing an output at +1 Vdc level in accordance with Mode 5 of Figure 3(e).As shown in Mode 6 of Figure 3(f), the zero-level voltage is created by switching on the switches T9 and T10 or off the power switching semiconductors in the inverter. T5, T7, and T8 are used to link the voltage at the input (-Vdc2 = - Vdc) to the load for -1 Vdc

level output, as shown in Mode 7 of Figure 3(g). As illustrated in Mode 8 of Figure 4 (h), T1, T5, and T8 are utilized to connect the input voltage (-Vdc1 -Vdc2 = - 2Vdc) to the load for -2Vdc level output. In a similar manner, negative voltage levels are produced, and Figure 4 shows a number of modes with circuit pathways.

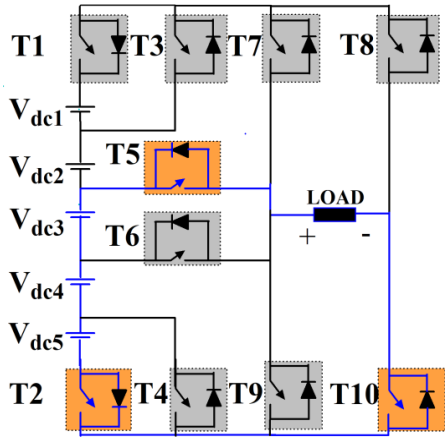


(a) Mode 1: +5Vdc

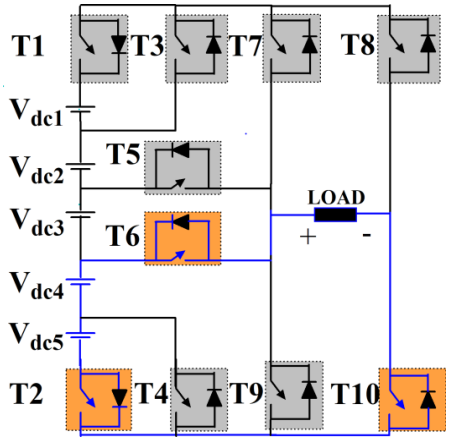


(b) Mode 2: +4Vdc

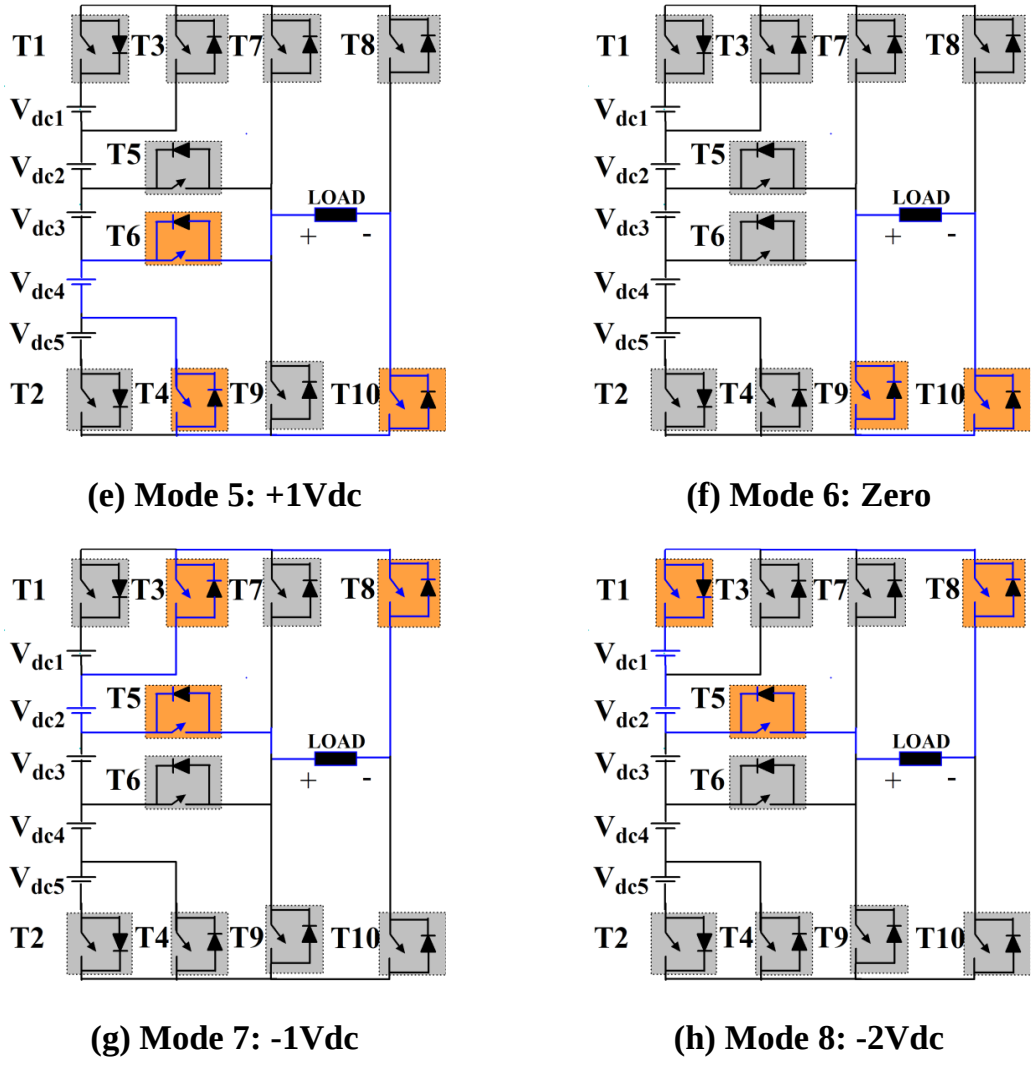
Figure 4 (Continued)



(c) Mode 3: +3Vdc



(d) Mode 4: +2Vdc



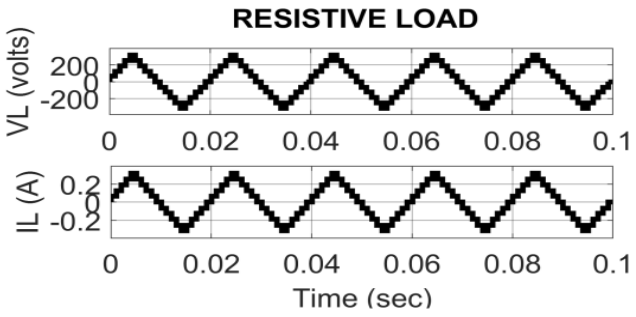
(e) Mode 5: +1Vdc **(f) Mode 6: Zero**

(g) Mode 7: -1Vdc **(h) Mode 8: -2Vdc**

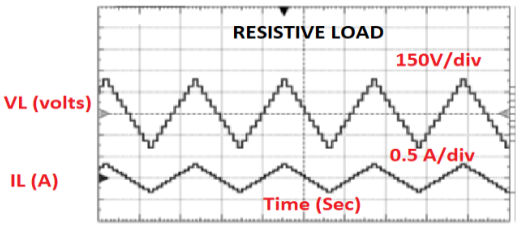
Figure 3 Various operating modes for the 10S-11L MLI are shown in Table 3.1 (Modes 1 through 8).

Total Harmonic Distortion (THD)

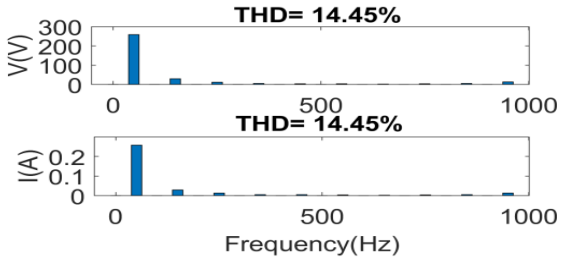
When attempting to synthesize the output voltage of MLIs, the normalized approach is most usually used. Most often, the waveform generated by the MLI is examined using the Fourier series growth approach. The MLI's output voltage has a quarter-wave waveform and is symmetrical. With a quarter-wave regular output, even-order harmonics are absent. Only angles between 0 and 90 degrees allow for switching. Analyzing the output voltage waveform of the proposed 10S-11L MLI is done with the goal of minimizing the harmonic content.



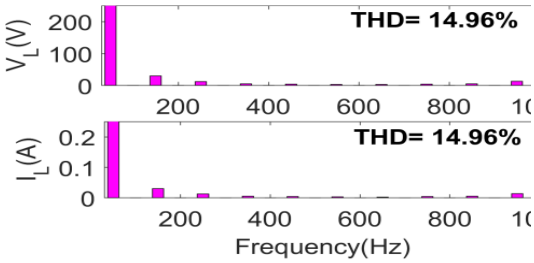
(a) Output voltage and current for a resistive load that is simulated (left; R = 1000 ohm)



(b) R = 1000 ohm resistive load output voltage and current

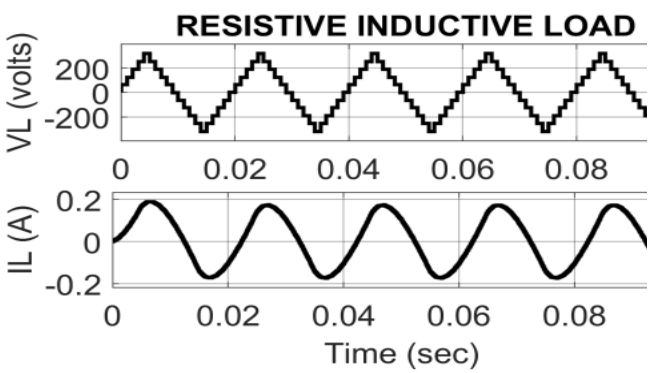


(c) FFT simulation for output voltage and current

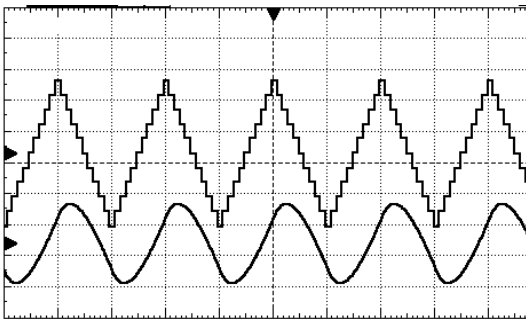


(d) output voltage and current FFT analysis

Figure 4 Results of 10S-11L single-phase symmetrical MLI with a resistive load (R = 1000 ohm) with random switching angles

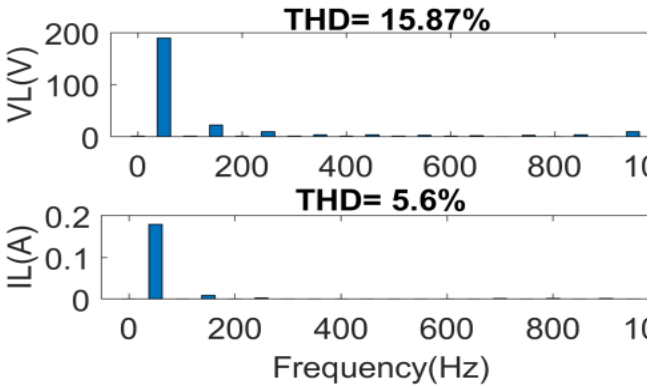


(a) Simulated output voltage and current for Resistive Inductive Load

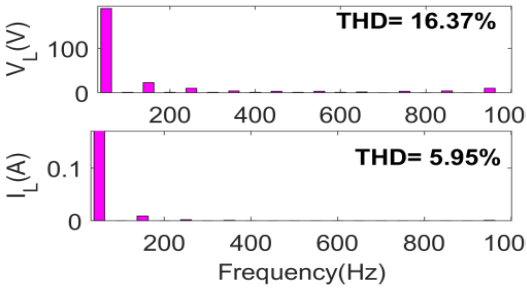


(b) output voltage and current for a resistive inductive load (R =

1000 ohm & L = 30 mH) were experimented



(c) FFT simulation for output voltage and current



(d) FFT analysis for output voltage and current

Figure 5. Results for random switching angles for the 10S-11L single-phase symmetrical MLI (R = 1000 ohm & L = 30 mH)

CONCLUSION

The recommended N-level symmetrical multilevel inverter system is designed to function with both resistive and resistive-inductive loads in order to meet the switching needs and address the problem encountered in a real-world scenario. The proposed 10S-11L MLI's design characteristics are 1000 ohms of resistance and 30 mH of inductance. The direct current sources in the simulation circuit each output a voltage of 65V. The inverter output frequency (Fm) is expected to be 50 Hz, whereas the switching frequency (Fs) is meant to be 4000 Hz. The simulated and tested THD analysis for an 11-level inverter reveals values of 14.45% and 14.96% when using resistive load and 15.87% and 16.37% when using resistive-inductive load when switching is performed on a regular basis without active filtering. Individual voltage distortion for 69KV systems should be less than 3%, and total harmonic distortion should be fewer than 5%, according to IEEE standard 519-2014. Harmonics are minimized in the proposed system by using multi-carrier PWM and normalized switching.

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