THD comparison of five, seven and nine level inverters using SPSS's data visualization technique

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Abstract- Multi-level inverters (MLI) are used widely in the recent years for high speed applications. Whenever high output is required to drive adjustable speed drives and certain variable speed drives, multi-level inverters are incorporated in the circuit. This paper presents MATLAB/SIMULINK models of five level, seven level and nine level inverter topologies. Cascaded H bridge topology is chosen for analysis. Five, seven and nine level inverter topologies are compared and output voltages are recorded. Further, total harmonic distortion THD is calculated for these topologies and results are tabulated. Total harmonic distortion comparison is done using data visualization tool to visually depict and understand there is a reduction in total harmonics with the increase in levels of the inverter.

Keywords:
***Index Terms*— Multilevel Inverter, Cascaded H bridge multilevel inverter, Insulated gate bipolar transistor, Total harmonic distortion, Statistical package for social science.**

I. INTRODUCTION

There are various topologies of multilevel inverters. Cascaded h-bridge multilevel inverter (CHBMLI) is widely used among the other topologies. CHMBLI uses less number of components and produces high quality output, very close to the sine wave. It is more suitable for photovoltaic applications [2].

Multilevel inverters mainly aim at operating in high voltage applications. It is used to operate mills, conveyors, pumps, fans and blowers [1]. Also, MLI also finds low power application in renewable energy sources. A multi-level inverter is variedly used in transportation, industrial manufacturing, and machine drive and as Staticvar compensator, which classifies its use extended to power systems, drives and aerospace as well. Using, multilevel inverters, dv/dt stresses are reduced on the semiconductor switches [7] and hence voltage stress also divides at different levels. As, we achieve multiple level output waveform, low THD is attained and power quality is improved [1]. Fault tolerant operation is established using suitable control schemes. When, we cascade multilevel inverters, it has the capability to high output voltage with higher reliability. As we increase the inverters to be cascaded in series, output drastically increases and reaches the required level as expected.

Further, total harmonic distortion estimation for each topology and each voltage level has to done in order to observe that cascaded topologies produce lower THD value with increase in the output voltage. Comparison of topologies and their performance is based on THD values. Further, we use data visualization tool SPSS to visualize the compared data [16].Various charts are available to visualize the recorded results in SPSS.A few selected representations are interpreted using pie charts, bar charts.

II.RELATED WORK

Inverters are widely used for adjustable speed drives; induction heating, Uninterruptible power supplies [18], and hvdc transmission lines [14]. MLI are generally used for high voltage, high power applications [11].Power quality improvement is also a main aspect for choosing multilevel inverters [1].

Depending on the type of Dc source incorporated, MLIs are classified under different topologies [4].Multilevel inverter topology chosen for analysis in this work is cascaded H Bridge .This topology is chosen as it produces low THD, easy to store, stress is reduced and limited [5].Harmonics are reduced to great extent [3].DC voltage levels are added together to form multilevel inverter topology (MLI).As a result of this smoother output waveform with fewer harmonic is achieved [6].Another advantage of using this topology is that it eliminates use of capacitor and diode, which in turn reduces switching losses and hence cost[5].

Five level, seven level and nine level inverters were simulated and output voltage waveforms were recorded. THD is calculated for the inverters chosen, where results indicate that THD reduces with increase in output voltage [12].This eliminates requirement of bulky transformers in the circuit[15].CHBMLI topology is chosen for comparison [8].

III.FIVE-LEVEL INVERTER

When H bridge inverters are connected in series, they produce a output voltage which is the sum of voltages generated by each cell. Numbers of voltage levels are 2n+1, where n denotes the number of cells. Number of components used in cascaded H bridge inverter is less compared to other topologies. N level cascaded H bridge multilevel inverter requires 2(n-1) switching devices where n denotes the number of output voltage level. The topology of five level inverter is discussed below in figure 1 with switching sequence in table I.

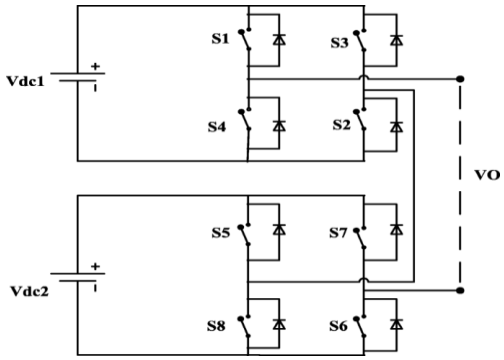

Fig. 1.Five level inverter CHBMLI topology.

The advantage of this method is that we do not require any capacitor or diode for clamping.Output is sinusoidal in nature. Output waveform filtering is not necessary as the level increases [6].Figure 2 represents the five-level inverter using 8 IGBT switches.

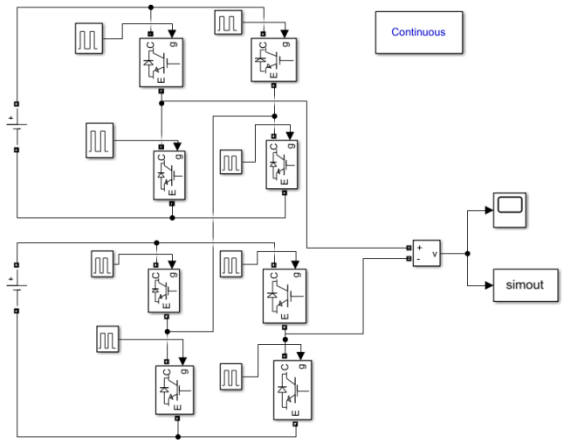

Fig.2.Five-level inverter MATLAB/SIMULINK model

IV.SEVEN LEVEL INVERTERS

Seven level six switch configuration is a unique configuration, it consists of six IGBT /DIODE switches. There is a switch across the load to maintain zero level. Figure 3 represent the seven level inverter with 6 switches.

Same configuration with R load is again repeated and waveforms are obtained. Figure 4 shows the 7 level inverter with R load. There are 7 levels of output voltages Vdc, 2Vdc, 3Vdc, 0.-Vdc,-2Vdc,-3Vdc [8].

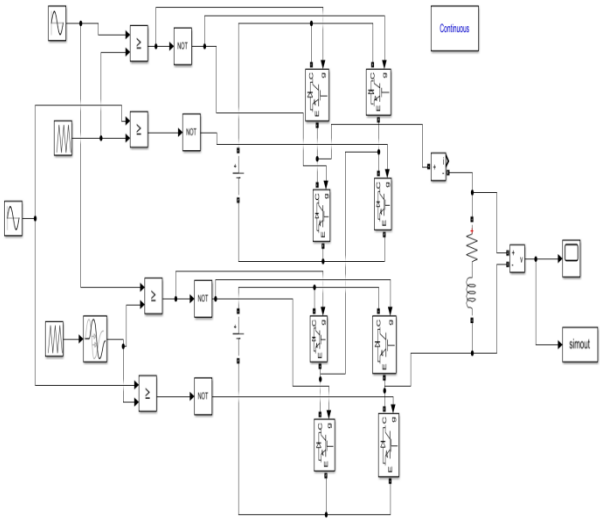

Fig.3.Seven-level inverter MATLAB/SIMULINK model RL Load

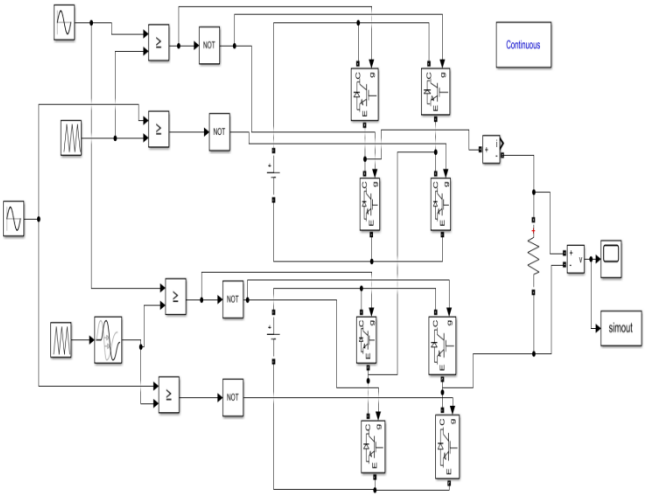

Fig.4..Seven-level inverter MATLAB/SIMULINK model R Load

V.NINE LEVEL INVERTER

Cascaded means inverters are connected in series, so four single level combine to form a full H bridge 9 level inverter. Each single bridge of the full bridge inverter produces +Vdc, 0,-Vdc [3].Total output voltage is the sum of voltages of each bridge. There are 16 switches in a nine level inverter [4].Nine level inverter rate of change of voltage is Vdc/4 to reduce switching loss.

The output voltage level for nine level cascaded inverter are +Vdc,+3Vdc/4,2Vdc/4,+Vdc/4,0,-Vdc/4,and-2Vdc/4,-3Vdc/4,-Vdc/4 according to the switching sequence presented in table I.

TABLE I. SWITCHING SEQUENCE

Output voltage	***Switching sequence***
Vdc/4	S1,S2,S5,S7,S9,S11,S13,S15
2Vdc/4	S1,S2,S5,S6,S9,S11,S13,S15
3Vdc/4	S1,S2,S5,S6,S9,S10,S13,S15
Vdc	S1,S2,S5,S6,S9,S10,S13,S14
0	S1,S3,S5,S7,S9,S11,S13,S14
-Vdc/4	S3,S5,S5,S7,S9,S11,S13,S14
-2Vdc/4	S3,S5,S7,S8,S9,S11,S13,S14
-3Vdc/4	S3,S5,S7,S8,S11,S12,S13,S14
-Vdc	S3,S5,S5,S7,S11,S12,S15,S16

Table I gives a clear picture of the 9 level CHBMLI

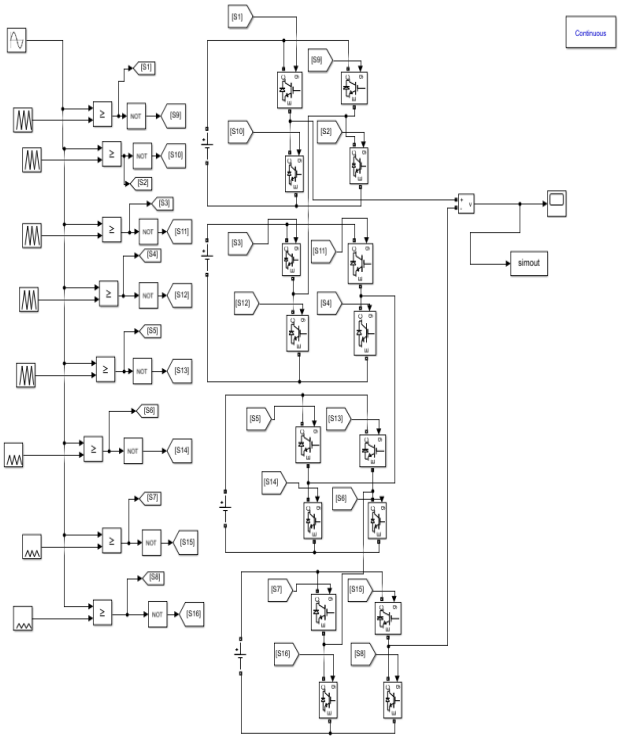

Fig.5. SIMULINK model of CHBMLI nine-level inverter

Figure 5 shows cascaded H bridge nine-level inverter simulated using MATLAB/SIMULINK

VI.WAVEFORMS AND RESULTS

The output voltages were recorded. Figure 6, 7, 8 and 9 shows the output voltage waveforms of five, seven and nine level inverters respectively. Total harmonic distortion was calculated for five, seven and nine level inverters using FFT analysis tool in MATLAB. [17] Figure 10, 11, 12 and 13 shows the THD of these inverters.

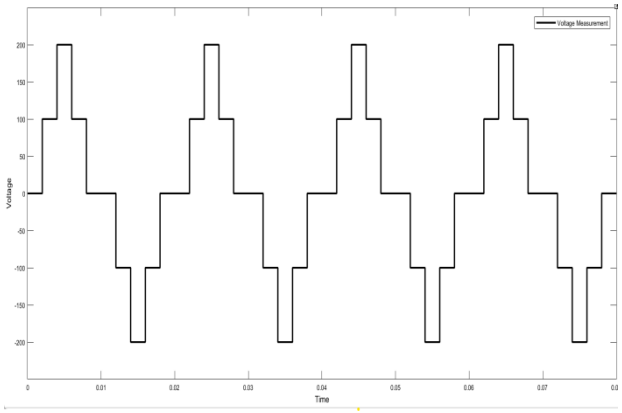

Fig.6.Output voltage waveform of five-level inverter

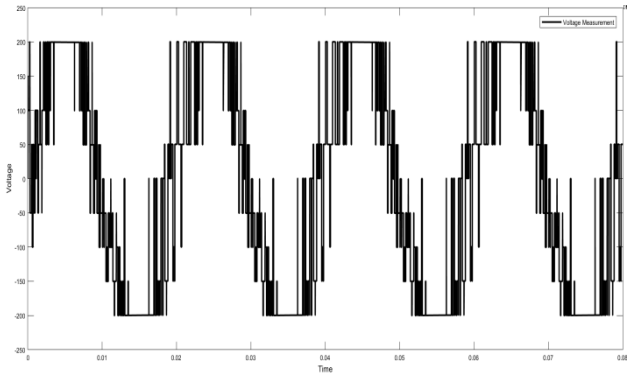

Fig.7.Output voltage waveform of seven-level inverter RL load

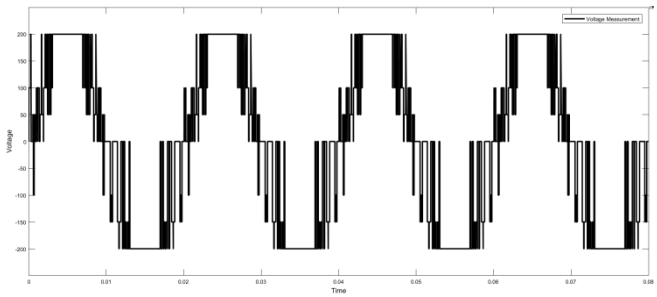

Fig.8.Output voltage waveform of seven-level inverter R load

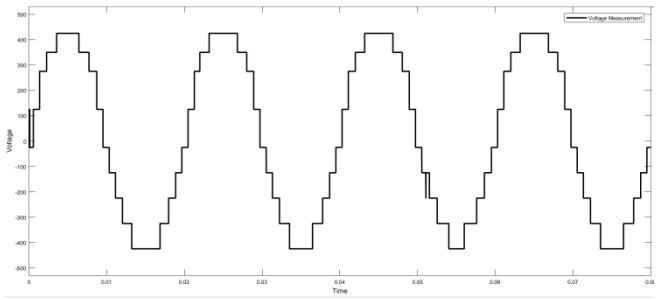

Fig.9.Output voltage waveform of nine-level inverter

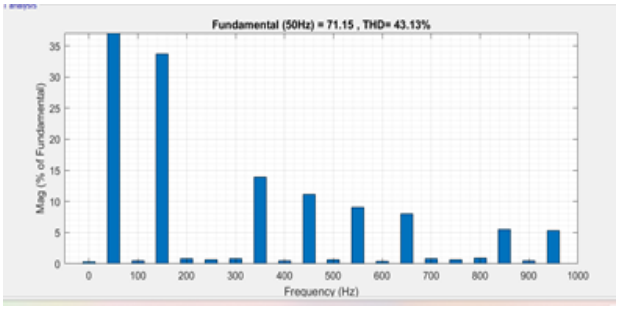

Fig.10.Total harmonic distortion of five-level inverter

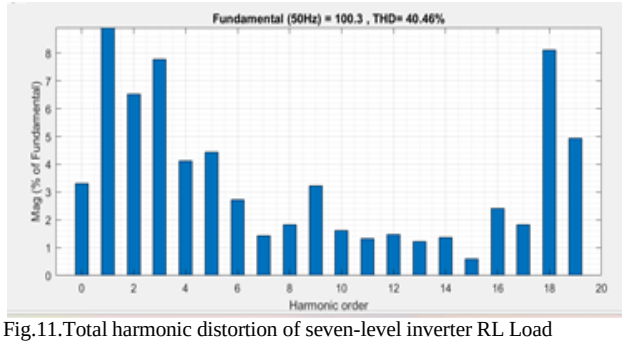

Fig.11.Total harmonic distortion of seven-level inverter RL Load

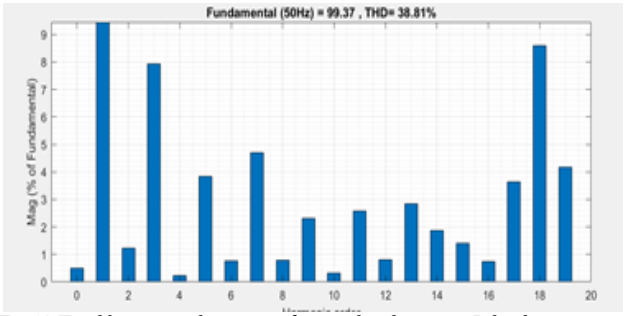

Fig.12.Total harmonic distortion of seven-level inverter R load

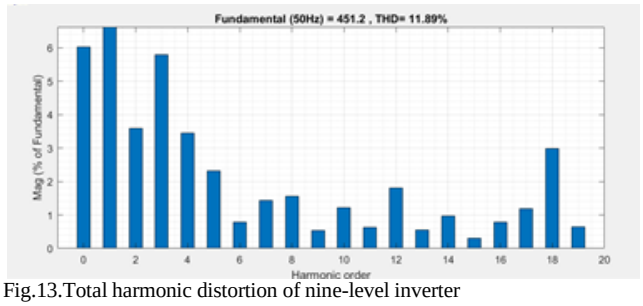

Fig.13.Total harmonic distortion of nine-level inverter

The results indicate that harmonic distortion reduces as the level increases [5]. The tabulation below shows the THD levels for five, seven and nine level inverter topologies.

TABLE II. THD COMPARISON OF FIVE,SEVEN AND NINE LEVEL INVERTERS

Level	***Frequency***	***Switches***	***THD***
Five	50 Hz	8	43.13%
Seven RL Load	50 Hz	8	40.46%
Seven R load	50 Hz	8	38.81%
Nine	50 Hz	16	11.89%

Table II clearly classifies the levels of the inverter, number of switches used in each inverter and also THD calculated**.**

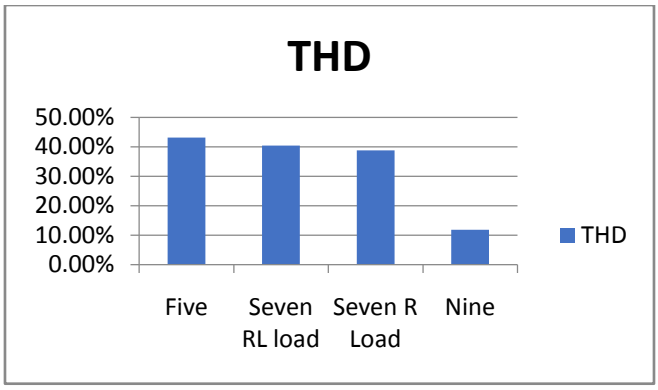

Fig.14.Total harmonic distortion comparison chart

The above Figure 14 shows THD comparison chart which clearly depicts that harmonic content reduces as the level increases.

Using data visualization tool statistical package for social science (SPSS), the total harmonic distortion for various levels are classified using chart builder .Figure 15, 16 and 17 shows different representation of level versus THD.

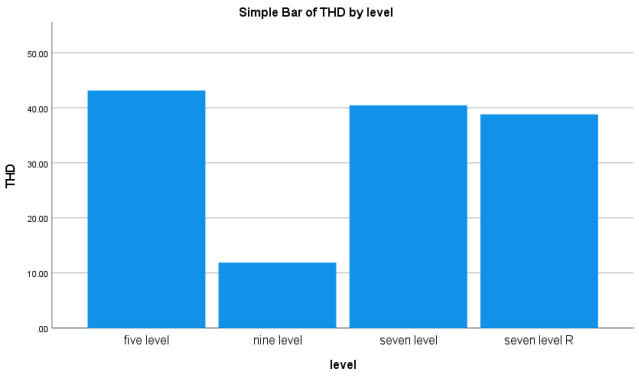

Fig.15.Bar chart representation of levels versus THD using SPSS

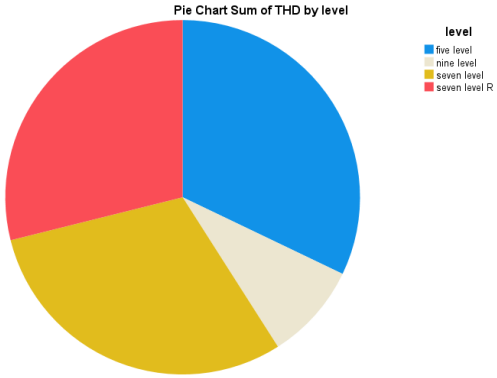

Fig.16.Pie chart representation of levels versus THD using SPSS

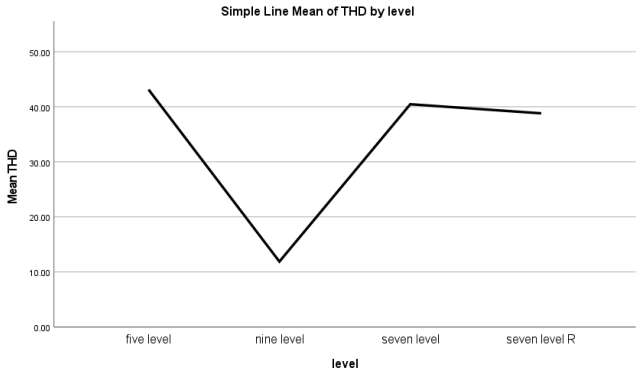

Fig.17.Line graph representation of levels versus THD using SPSS

The above graphs and charts indicate decrease in THD with the increase in levels of the inverter.

Apart from comparing the THD values, statistical analysis of the THD calculated for above inverters are represented as figure 18 below.SPSS is a powerful statistical tool used for calculating mean, mode, median and standard deviation of a given data set.In this research, we have the recorded data set of THD values of various inverters.SPSS calculates the above parameters for the recorded data. Table III contains the numerical data of calculated statistical parameters.

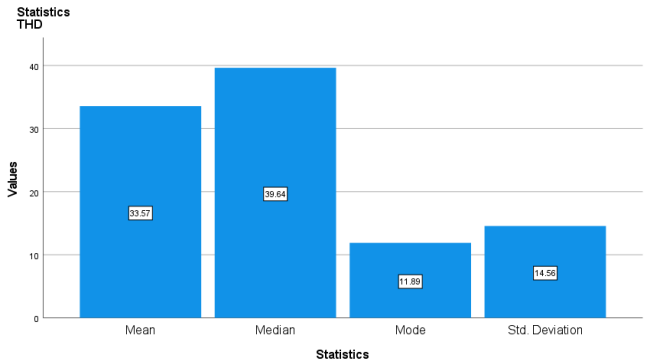

Fig.18.Statistics of THD values of inverters

TABLE III. STATISTICS OF THD

Parameter	***Value***
Mean	33.57%
Median	39.64%
Mode	11.89%
Standard deviation	14.56%

VII.CONCLUSION

With the advent of high speed applications, multilevel inverters are widely used for many applications. Furthermore, whenever high output is required to drive the load, MLI are preferred [7].Comparison of multi-level inverter topologies based on THD is done. Results clearly demonstrate that as the level increases, output voltage increases and hence total harmonic distortion reduces. Data visualization tool plays a vital role in depicting the compared values and gives a clear picture of reduction in THD. SPSS tool is used to calculate the statistical parameters of the THD values and again that is visualized as charts.

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