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A novel discrete 3-phase PWM generator design & simulation for a 3-phase, 4-level inverter to mitigate harmonic distortions in industrial power converters

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Abstract

In this paper, a novel discrete 3-phase PWM generator design & simulation for a 3-phase, 4-level inverter to mitigate harmonic distortions in industrial power converter is presented along with its simulated results. Design is conducted in the Simulink' of the Matlab environment. The result are compared with others to show the efficiency of the methodology that has been developed by the team of researchers. This paper presents a novel design for a discrete 3-phase Pulse Width Modulation (PWM) generator, which is utilized in the simulation of a 3-phase, 4-level inverter to mitigate harmonic distortions in industrial power converters. The proposed PWM generator design achieves superior harmonic suppression compared to conventional PWM techniques, making it suitable for use in a wide range of industrial applications. The simulation results demonstrate the effectiveness of the proposed design in reducing the total harmonic distortion of the inverter output voltage waveform. The presented approach offers a practical solution to enhance the performance of industrial power converters in terms of harmonic suppression, and has the potential to be applied in various power electronic systems.

Keywords Power, FACTS, Inverters, Phase, Harmonics, Mitigation, Simulink, Model.

Introduction

PE converters play a vital role in modern PSA and industrial applications. However, their operation often leads to the generation of harmonic distortions, which can have detrimental effects on power quality and cause significant losses in the system. Pulse Width Modulation (PWM) techniques are commonly used to mitigate these distortions. In this context, this paper introduces a novel discrete 3-phase PWM generator design that is used in the simulation of a 3-phase, 4-level inverter to reduce harmonic distortions in industrial power converters. The proposed design offers improved harmonic suppression compared to conventional techniques and has the power for enhancing the performances of power electronic system in various applications [20].

Review of Literature

A number of researchers have worked on the proposed topic & here follows a brief review of the works done by various research community people. Zainal Salam et al. conducted a brief literature review on active power filters for harmonic mitigation, covering various techniques that use power sc's. This survey paper provided a foundational understanding of harmonics, their effects, and potential elimination methods. Suves Vore and Dipek Bhett presented a comprehensive' reviews of the effect of harmonics on electrical power's qualities, while Arrillaga et al. gave a general review of harmonics in an IEEE paper. Yogesh et al. reviewed the reductions of harmonic using FL controllers with active filters. Additionally, Leszek S. Czarnecki provided an exhaustive summary of harmonics suppressions methods in distribution system in their review paper, and Imtiaz Ahmed et al. gave a detailed overviews of harmonics source in power-systems, providing a valuable source of knowledge [1].

While effective for linear loads, the approach discussed in previous work had a major drawback when it came to non-linear loads. Ming-Yin Chan et al. conducted case study surveys of harmonic currents generated by computers in an office building and found that extensive computer use created significant harmonics, cross-talks, and misfires, which caused power fluctuations, radio interference, and equipment malfunctions. They concluded that harmonic currents were the culprit and conducted a brief analysis on the subject. Fergusen directed his attention towards enhancing power quality in a harmonic environment. He developed a strategy that employed power semiconductor devices to enhance power factor in the supply system. Nevertheless, despite the

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use of such devices, complete elimination of total harmonic distortion was unattainable. This was primarily due to the switching devices being produced by various manufacturers with identical ratings [2].

The importance of stability in ensuring the quality of power supply was highlighted by the authors, who also presented methods to improve stability using power electronics devices. However, their approach was found to be inadequate for high loads, such as those found in industrial settings, leading to frequent power outages. Narain Hingorani's well-known textbook provides a comprehensive introduction to harmonic analysis, reduction techniques, and power quality improvement. Similarly, Alexander Kusov's renowned textbook provides theoretical insights into power quality, covering topics such as design, modeling, and practical applications. In any harmonic reduction strategy, cost must be considered a critical factor during the design and development of the harmonic reduction system [3].

Aredas etal. devised new controlled strategy for a 3-ph 4-wired shunt actived filter (LC with power electronics devices) to mitigate harmonic in the papers. Zhen etal. proposed an algorithm for PWM and demonstrated that it could partially suppress harmonics in interconnected grid power systems. A team of researchers, Dai et.al., formulated a FPGA, which yielded favorable results in reducing harmonics. In their work, Jou et.al. conducted an extensive analysis of the use of zig-zag transformers in 3-phase 4-wire distribution power systems to study the effect of harmonics in power electronic based systems [4].

Their work proposed a Shunt Actived Filters (SAF) using the Variables Indexed Pulses Width Modulated approaches. In their PWM method, the reference signals were integrated to derive the triangular wave, and their results demonstrated that their approach satisfied the IEEE-519 standard for harmonics reduction. Lian, Perkins, and Lehn presented a time domain method for analyzing the three-phase rectifier with capacitor output filter in their published work. Their proposed method analytically evaluated harmonics and obtained exact switching functions through iterative solving for the switching instants, resulting in significant harmonic reductions [5].

Shwehdi and Ismail conducted a study on the effects of harmonics produced on line currents in university personnel computers (PCs). Their research, published in a journal, revealed that harmonics can adversely affect the performance of PCs. They developed a neuro-fuzzy scheme for harmonic suppression and conducted a tradeoff analysises amongst various intelligent controlled based resistive emulated technique, using the concepts of Artificial Neural Networks. Sam AbdelRahma PFC's boosted converters designs guided by Infineon can serve as a handbook for the design of power electronics circuits, including a comparison between traditional PI controller-based active resistance emulation and FLC & ANFIS depended controllers emulation [6].

A comparison of current ripples and THD was conducted using MATLAB/Simulink simulations and the results were tabulated. The proposed method demonstrated significant effectiveness, as evidenced by the simulation results. In their research work, Mridul & Dubey presented a novel NF dependent control strategy for a three phase 4-wire shunt actived powered filters, which enhanced the dynamics of the APF to minimizing harmonic for a larege range of load current variation and various conditions. Alham Hassan et.al. developed advanced solutions to power quality problems by solving all the issues related to passive L-C filters [7].

Researchers such as Satheeswaran, Suresh Kumar, and Bhim Singh have made significant contributions to reducing power quality harmonics caused by switching devices through various schemes, many of which have been effective in industrial sectors, albeit limited to nonlinear loads. As the use of inverters in power systems grew, injected harmonics became a critical problem that deteriorated the power quality. Inverter requirements in integrated power systems and micro-grids highlighted the need for achieving low distortion and efficient power exchange through inverters [19]. The review papers discussed provide an adequate introduction to the fundamental principles of filter design and implementation, which can aid researchers in their work. Additionally, a comprehensive text written by Holmes D.G., Lipot A. and published by the IEEE is an excellent resource for understanding the generation of signals for inverters and converters used for harmonic reduction in power systems [8].

Design of Four stage/level voltage-bolstered PWM inverters

Multi-megawatt industrial drive applications have seen a surge in popularity of four-level voltage-boosted PWM inverters [18]. This is attributed to the convenience of sharing high voltage among arrangement devices and the improved harmonics qualities at the outputs compared to a 2-levels inverter used in dual cascade with specific circuit design modifications. In the realm of lower power range, IGBTs are replacing GTO devices due to their higher switching frequency and rapid development in voltage and current ratings. Additionally, utilizing SV - PWMs technique in a four-level inverters offers the added benefits of superior harmonics qualities and a large under-balance range, which can extend the stability factor to 95% from the conventional value of 75% in Sine based Pulse Width Modulation [9].

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The principle of operation of each level of the inverter can be explained as follows. For a 3-phase inverter, a 6step SCR bridge is used, with 6 switches, 2 switches for each phase. Each step represents a change in the operation time of each transistor to the next transistor, defined in a proper sequence. In a 6-step inverter, each step is a 60-degree interval for a cycle of 360 degrees. A higher level can be achieved with a 3-phase bridge inverter using 6 IGBTs. By paralleling four 6-pair switches, a 40-level inverter can be formed. In this circuit, large capacitors are connected at the input terminals to maintain constant DC input and suppress the harmonics fed back to the source [17]. There are two transistor gating patterns used in the bridge unit. In one pattern, each transistor conducts for 180 degrees, and in the other pattern, each transistor conducts for 120 degrees. Gating signals are applied and removed at an interval of 60 degrees of the output voltage waveform for both patterns. As the number of levels increases, isolation effects must be considered, which can be addressed by using properly designed 3-phase transformers [10].

Specifications of the model

The simulation model used in this study has the following specifications: a 10 KW, 3-phase, 50 Hz, 100 V, 4level inverter, with a 4-thyristor bridge and a 100 V DC source. Levels 1 and 3 use multiple thyristor bridges, while levels 2 and 4 use IGBTs coupled with diodes. As a result, two levels work with SCRs, and the other two levels work with IGBTs and diodes. This converter effectively suppresses harmonics resulting from the on/off switching of loads [11].

Model of Simulink – Development

Model of simulink is created by utilizing different types of blocks with a no. of components [12].

- The simulation time can vary from 0.1 to 10 seconds.
- A discretization purpose time of 1 ms is used in the simulation.
- The FFT analysis is performed on the penultimate cycle of signals.

The results obtained from the frequency analysis reveal a significant reduction in the harmonic content, leading to a notable improvement in power quality by almost five times compared to the 2-level model. The output signals from the inverter (phase A) and load output voltages are observed, and the set value in designs are reflected in the o/p waveform, which are approximately 100 Volts [13].

Block Parameters: S	CR BRIDGE 1		>
Three-Level Bridge (mas	() (linik)		
devices. Series RC snub	hree-level bridge of selected f ber circuits are connected in p ber values when the model is o	arailel with each switch de	
Parameters			
Number of bridge arms:	3		*
Snubber resistance Rs ()	Ohms)		
1e10			
Snubber capacitance Cs	(F)		
inf			
Power Electronic device	Ideal Switches		
Internal resistance Ron	(Ohms)		
1e-10			
Measurements None			
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		5 m

Fig. 1 : Configuring the blocks parameter in the first SCRs / Thyristor Bridges.

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Sou	rce Block Parameters: Pulse generator 1	>
Discret	e 3-phase PWM Generator (2- or 3-level) (mask) (link)	
Pulse V forced- using a output Jse ou signals	crete 3-phase PWM Generator block generates pulses for carrier-based /idth Modulation (PWM) converters. The block can be used to fire the commuted devices (FETs, GTOs, or IGBTs) of 2-level or 3-level converters single bridge or two bridges connected in twin configuration. Vectorized a P1 and P2 contain either 6 pulses (2-level) or 12 pulses (3-level). tput P1 when operating in single-bridge configuration. The modulating can be applied at Input 1 (UreF) and the synchronization signal at input 2 inter the mask' of the block to get a description of the pulse pattern.	
Parame	ters	
Type	3-level	4
Mode of operation Un-synchronized		*
Carrier	frequency (Hz):	
10000		
🗹 Int	ernal generation of modulating signal(s)	
Module	ition Index:	
0.95		
Outpu	t voltage frequency (Hz):	
Outpu	t voltage phase (degrees):	
0		
Sample	time:	

Fig. 2 : Configuring the parameters of the PWM pulse generator block to generate pulses for the inverter.

Block Parameters: 3-phase inductive load 1	×
Three-Phase Parallel RLC Load (mask) (link)	
Implements a three-phase parallel RLC load.	
Parameters	
Configuration Y (grounded)	-
Nominal phase-to-phase voltage Vn (Vrms)	
400	
Nominal frequency fn (Hz):	
50	
Active power P (W):	
1000e3	
Inductive reactive Power QL (positive var):	
1000	
Capacitive reactive power Qc (negative var):	
1000	
Measurements None	+
OK Cancel Help	Apply

Fig. 3 : The process of configuring the blocks parameter for the three phase RLC inductive loads that is connect to the system's o/p.

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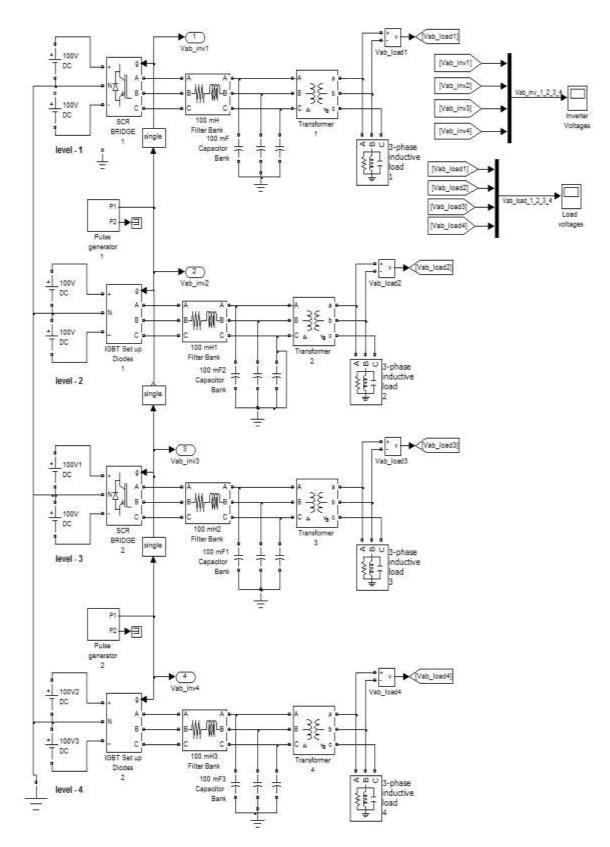


Fig. 4 : Model which includes thyristor bridges, filter banks, and harmonic elimination circuitries to improve power quality

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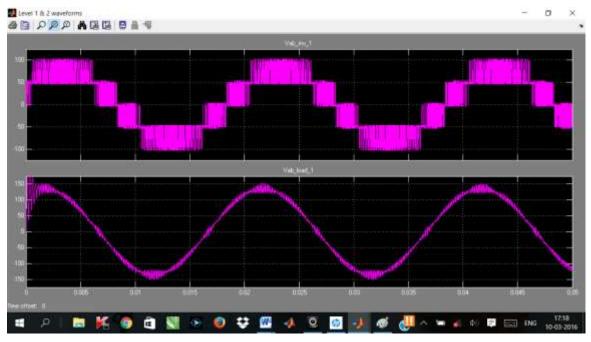


Fig. 5 : Waveform 1.



Fig. 6 : The waveforms of the combined levels 1 and 2 for the inverter output and load output are displayed, show harmonics content along with un-distorted supply's waveform, which have been zoom in.

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Fig. 7 : The o/p waveforms of the combined levels 1 and 2, including inverter output and load output, demonstrate a smooth output supply after the incorporation of the filter, resulting in the removal of all harmonics up to the 8th order.

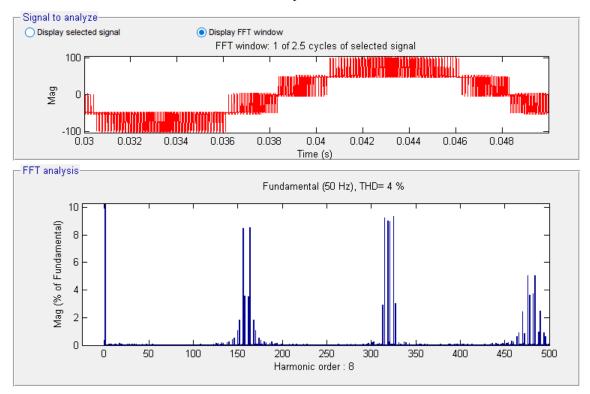


Fig. 8 : Frequency analysis of load 1's supply voltage using FFT

Parameter	3-¢ 2-level	3-¢ 4-level
Modulation index	0.95	0.95
THD	22 %	4 %
Magnitude	100 units	10 units

Table 11 : Analysis to compare the performance of the harmonic elimination systems between 2-level and 4level configurations

The fifth figure shows the output waveforms of the combined levels 1 & 2 before the filter integration, whereas the sixth figure displays the same output waveforms, zoomed in to show harmonic contents and undistorted supply waveforms. The seventh figure demonstrates the output waveforms after the incorporations of the filters, resulting in smoothened output supplies using complete harmonic removal up to the 8th order [14].

The multi-stage hybrid design of the system has several advantages. Compared to 2-level inverters, multilevel inverters have significantly reduced harmonic distortion, which was demonstrated through novel simulations conducted in the Matlab-Simulink environment. Additionally, THD reduction tables were created for both current and voltage, and the THD for the o/p waveform is found using THD's formula [15].

It has been observed that it reduces TDH from 22% to 4%, while desirable voltage and frequency have been achieved. The comparison between the results of the 2-level and 4-level systems indicates good performances. Furthermore, the output voltage waveform appears more sinusoidal as the level increases, which is also supported by the FFT analysis of the voltage signals [16].

Sr. No. Type of harmonic elimination method	THD Before Harmonic Suppression (Load v)	THD After Harmonic Suppression (Load v)	THD Before Harmonic Suppression (Load i)	THD After Harmonic Suppression (Load i)	Power Factor	Remarks
Sr. No. 5 36 4 level Inverter	0.4102 41.02 %	0.0401 4.01 %	0.3126 31.26 %	0.0305 3.05 %	0.91	IV
Sr. No. 4 3-\$, 2-level inverter	0.7204 72.04 %	0.2224 22.24 %	0.5234 52.34 %	0.0655 6.55 %	0.85	VIII Least

Table 2 : The parameters of a 3-phase 2-level inverter are being compared.

Conclusions

The paper presented a new design and simulation for a 3-phase, 4-level inverter aimed at mitigating harmonic distortions in industrial power converters. The study delved into several aspects, such as the inverter design, working standards, and neutral point voltage control, among others. The 3-ph 4-level 6-switches inverter was simulated, and its performance was improved by using a modulation control plan to generate anti-harmonic signals to neutralize them. Unlike the traditional 4-stage inverter. The research concludes that the use of 4-level inverters outperforms the 2-level inverter when it comes to reducing the harmonic components of the output voltage, and it provides better performance compared to previous studies. Additionally, the paper explores the space vector regulation procedures, although they are not incorporated for the sake of convenience.

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