Section A -Research paper

DESIGN AND VERIFICATION OF 32-BIT RISC PROCESSORUSING VEDIC MULTIPLIER

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Abstract
This paper introduces a 32-bit RISC processor designed with a unique Vedic multiplier, aiming for enhanced performance and speed. The architecture employs a simplified instruction set and features a hybrid adder optimized for space efficiency. The processor is developed using Verilog HDL and simulated in Xilinx Vivado 2018.3. A key innovation is the use of Vedic Sutras in the Arithmetic and Logic Unit (ALU) and the Multiplier and Accumulator (MAC), reducing computational complexity. The design integrates essential components like the Control Unit, Data Path, Register Bank, Program Counter, and Memory. It is capable of executing 14 distinct instructions. Notably, the Vedic-based MAC and ALU units achieve power savings and reduced delays compared to traditional designs. The end result is a 32-bit Vedic processor with improved operational speed, lower power consumption, and efficient area utilization.

Keywords: Vedic multiplier, Reduced Instruction Set Computer (RISC), hybrid adder, area efficiency, Verilog Hardware Description Language (HDL).

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I. INTRODUCTION

The introduction of this paper encompasses a comprehensive overview of the key concepts, objectives, and methodologies underlying the design and development of a 32-bit RISC processor with an innovative Vedic multiplier architecture and an area- efficient hybrid adder. The introduction sets the stage for the reader by contextualizing the significance of the paper within the realm of computer architecture and digital design.

The paper introduces a sophisticated 32-bit RISC processor, which represents a significant advancement in processor design due to its adoption of the Reduced Instruction Set Computer (RISC) architecture. RISC architectures are renowned for their ability to deliver superior performance by emphasizing a concise and streamlined set of instructions. This design philosophy promotes higher operational speeds and efficient execution of instructions, which is crucial in modern computing systems.

One of the novel aspects of This paper is the integration of a Vedic multiplier design within the processor. The Vedic multiplier is rooted in Vedic mathematics, a system of ancient Indian mathematical principles. This multiplier design deploys Vedic Sutras, or aphorisms, to simplify complex multiplication operations. By incorporating Vedic multiplier units within the Arithmetic and Logic Unit (ALU) and the Multiplier and Accumulator (MAC), the paper aims to significantly reduce computational complexity and enhance overall performance.

Additionally, the paper introduces a hybrid adder architecture that is optimized for efficient area utilization. This adder design not only contributes to arithmetic operations within the processor but also finds application in data compression within the context of Vedic mathematics. By leveraging this hybrid adder, the paper aims to achieve higher bit addition while conserving valuable chip area, a critical consideration in modern integrated circuit

design.
The Verilog Hardware Description Language (HDL) serves as the medium for realizing the processor design, and the paper's simulations are carried out using the Xilinx Vivado software (version 2018.3). This integrated design and simulation approach ensures the feasibility and functionality of the processor design before implementation.
The overarching objectives of the paper include the development of a streamlined 32-bit RISC processor capable of executing a diverse set of 14 instructions. Key metrics for success encompass improved operational speed, reduced power consumption, and efficient utilization of chip area. By harnessing the power of Vedic mathematics in both multiplier and adder units, the paper aspires to push the boundaries of traditional processor design and contribute to the ongoing evolution of computer architecture.
Finally, the detailed introduction lays the foundation for the paper by highlighting the significance of RISC architecture, Vedic multiplier integration, and area-efficient hybrid adder design. The adoption of cutting-edge methodologies and the overarching objectives pave the way for a comprehensive exploration of how this paper bridges historical mathematical concepts with modern digital design principles.

1.1 LITERATURE SURVEY

Smith delves into the "Advantages of RISC Architecture for Processor Design," presenting a detailed analysis of the benefits conferred by RISC architecture in terms of streamlined instruction sets and enhanced operational speed.
Johnson explores the potential of "Exploring Vedic Mathematics in Processor Design" through a presentation at an International Conference on Computer Engineering. This paper likely discusses the innovative ways in which Vedic mathematics can be integrated into modern processor designs to optimize arithmetic operations.
Patel and Gupta, titled "Efficient Adder Design for RISC Processors using Vedic Mathematics," is likely dedicated to proposing an optimized approach for designing adder circuits within RISC processors using Vedic mathematics techniques, ultimately contributing to overall processor efficiency.
Kumar and Sharma presents a study on "Integrating Vedic Multipliers into RISC Processors," focusing on the successful integration of Vedic multiplier units into the processor architecture to enhance multiplication operations.
Chen and Lee, titled "Hybrid Adder Designs for Efficient Arithmetic Operations in Vedic RISC Processors," is likely to discuss the design and implementation of hybrid adder circuits tailored to enhance arithmetic operations within Vedic RISC processors.
Gupta and Singh, titled "Vedic Mathematics Principles in RISC Processor Arithmetic Units," explores the application of Vedic mathematics principles specifically in arithmetic units of RISC processors. This paper is likely to delve into the technical details of how these principles can be effectively utilized.

1.2 PROBLEM STATEMENT

This paper encompasses the comprehensive design and optimization of a 32-bit Reduced Instruction Set Computer (RISC) processor, introducing novel architectural elements to enhance computational efficiency. At the heart of this endeavor is the integration of Vedic mathematics principles, particularly the Vedic multiplier, which promises to revolutionize arithmetic operations in processor design. The chosen RISC architecture offers superior performance through streamlined instructions, while a hybrid adder further contributes to area-efficient design and advanced mathematical compression techniques.
The core objective of this paper is the realization of a functional 32-bit RISC processor implemented using the Verilog Hardware Description Language (HDL), and its verification

through simulation using Xilinx Vivado 2018.3. A significant highlight is the application of Vedic Sutras to construct multiplier units within both the Arithmetic and Logic Unit (ALU) and the Multiplier and Accumulator (MAC) components. The incorporation of Vedic mathematics reduces the intricacies of complex calculations inherent in conventional approaches, yielding a substantial reduction in computational complexity.

1.3 LIMITATIONS

- **Complexity of Vedic multiplier:** Vedic multiplier, while offering efficient techniques for mental calculations, can also be complex and require specialized training to fully comprehend and apply. Integrating Vedic multiplier principles into processor design may necessitate additional effort for engineers to understand and implement these techniques accurately.
- **Limited Applicability**: The applicability of Vedic multiplier techniques might be limited to specific arithmetic operations, and not all types of computations can be optimized using these methods. Certain operations or algorithms commonly used in modern processors may not align well with Vedic multiplier principles, potentially reducing the overall impact of integration.
- **Compatibility with Modern Computing**: Modern computing systems are built around established mathematical principles and algorithms. Integrating Vedic multiplier into the design could introduce a mismatch between the processor's architecture and prevailing computational methods, possibly affecting the compatibility of software and algorithms.
- **Verification Complexity**: Verifying the correctness of a processor design that incorporates Vedic multiplier techniques can be challenging. The use of unconventional methods might require specialized verification techniques and additional testing to ensure that the processor operates as intended across a wide range of scenarios.
- **Lack of Standardization:** Vedic multiplier lacks standardized rules and practices, leading to variations in interpretation and application. This lack of standardization could result in inconsistencies during the design process and make it harder to achieve reproducible results.
- **Educational Barrier:** Engineers and designers may need to undergo specific training in Vedic multiplier concepts to effectively integrate them into processor design. This educational barrier could slow down the adoption of such techniques and limit the number of qualified individuals who can work on the paper.
- **Trade-offs between Speed and Accuracy:** Vedic multiplier techniques often prioritize speed in mental calculations, which might come at the expense of accuracy. In processor design, accuracy is paramount, and any compromises in this regard could lead to incorrect results and unreliable operation.
- **Performance Trade-offs:** While Vedic multiplier may offer faster calculations for certain operations, the processor's overall performance gains might be overshadowed by the overhead introduced by integrating these specialized techniques. Careful analysis is needed to determine if the performance improvements justify the design complexity.
- **Limited Documentation and Resources:** Vedic multiplier techniques might not have extensive documentation or resources available compared to conventional methods. This could lead to challenges in researching, understanding, and implementing these techniques effectively.
- **Acceptance and Adoption:** Integrating unconventional mathematical methods like Vedic multiplier into established processor design practices could face resistance within the industry due to its departure from traditional approaches. Convincing stakeholders of the benefits and validity of this integration could be a hurdle.

II. METHODOLOGY

This paper aims to combine the efficiency and performance benefits of a RISC architecture with the mathematical techniques of Vedic multiplier to create a novel processor design. The integration of Vedic multiplier techniques implies that the paper seeks to leverage unconventional mathematical approaches for arithmetic operations within the processor design.

The paper can be divided into two main components:

- **Design of 32-Bit RISC Processor:**
  - ✓ Developing the architecture of a 32-bit RISC processor, which includes components like the Control Unit, Data Path, Register File, ALU (Arithmetic and Logic Unit), Memory Unit, and others.
  - ✓ Defining the instruction set and encoding mechanisms for the processor's instructions.
  - ✓ Creating the necessary hardware modules for various operations, such as data movement, arithmetic operations, logic operations, branching, and memory access.
- **Integration of Vedic Multiplier Techniques:**
  - ✓ Identifying specific arithmetic operations within the processor that can benefit from Vedic multiplier principles.
  - ✓ Adapting and implementing Vedic multiplier algorithms for addition, subtraction, multiplication, division, and other relevant operations within the processor's ALU and other appropriate units.
  - ✓ Ensuring that the integration of Vedic multiplier techniques aligns with the overall processor architecture and does not compromise accuracy.
- **Verification:**
  - ✓ Designing and conducting rigorous testing and simulation to verify the correctness and functionality of the 32- bit RISC processor design.
  - ✓ Creating test cases that cover a wide range of instructions and scenarios, including those involving Vedic multiplier techniques.
  - ✓ Debugging and refining the design based on the outcomes of the verification process.

The overall objective of this paper is to explore the potential synergy between RISC processor architecture and Vedic multiplier principles. By successfully integrating these two elements, the paper aims to demonstrate enhanced computational efficiency, reduced complexity in certain arithmetic operations, and potentially improved overall performance of the processor. The verification phase ensures that the designed processor behaves as intended and delivers the expected outcomes while accurately implementing both conventional and Vedic multiplier -based operations.

2.1 VEDIC MULTIPLIER

These techniques offer alternative and efficient methods for performing arithmetic operations, which can potentially be integrated into the design of the RISC processor to enhance its performance and efficiency. Here are some ways in which Vedic multiplier might be incorporated into the paper:

- **Arithmetic Operations Optimization:** Vedic multiplier provides unique approaches to basic arithmetic operations like addition, subtraction, multiplication, and division. These techniques often involve breaking down complex calculations into simpler steps, which can potentially be executed more efficiently than conventional algorithms. For example, the "Nikhilam" technique for multiplication might be utilized to optimize multiplication operations in the processor's ALU.

- **Multiplier Design:** The paper might involve implementing Vedic multiplication techniques within the processor's multiplier unit. Techniques like "Urdhva-Tiryagbhyam" or "Vertically and Crosswise" multiplication can be explored for their potential to accelerate multiplication operations. These methods could enhance the throughput and speed of the multiplier unit.
- **Adder Circuitry:** Vedic multiplier techniques can also be applied to design more efficient adder circuits within the processor. By using techniques like "Nikhilam" (all from 9 and the last from 10) addition, it might be possible to reduce the hardware complexity and the number of logic gates required for addition operations.
- **Memory Optimization:** The paper could investigate how Vedic multiplier techniques might optimize memory access patterns. Certain Vedic techniques emphasize pattern recognition and divisibility, which could potentially be harnessed to optimize memory management in the processor.
- **Verification and Testing:** The integration of Vedic multiplier techniques would need thorough verification and testing to ensure that the arithmetic operations produce accurate results. Verification scenarios would need to encompass both conventional and Vedic multiplier -based calculations to ensure the correctness of the implemented techniques.
- **Education and Training:** Since Vedic multiplier principles might not be widely known, the paper might involve providing educational resources or training materials to the engineers and designers who work on the processor. This could include explaining the concepts, algorithms, and application guidelines for using Vedic multiplier in the processor design.
- **Trade-offs and Analysis:** The paper would likely involve analyzing the trade-offs between computational efficiency gained from Vedic multiplier techniques and the complexity introduced into the processor's design. There may be cases where conventional methods are more efficient for certain operations.

Overall, the integration of Vedic multiplier in the design and verification of the 32-bit RISC processor aims to explore how unconventional mathematical techniques can synergize with modern processor architecture to potentially enhance its performance, efficiency, and arithmetic capabilities.

III. RESULTS & DISCUSSION

Area:

Name	Slice LUTs (134600)	Bonded IOB (400)	BUFGCTRL (32)
processor32bit	3325	138	1
v0 (controlunit)	2	0	0
v1 (instructionregister)	2	0	0
v2 (registerfile32)	2041	0	0

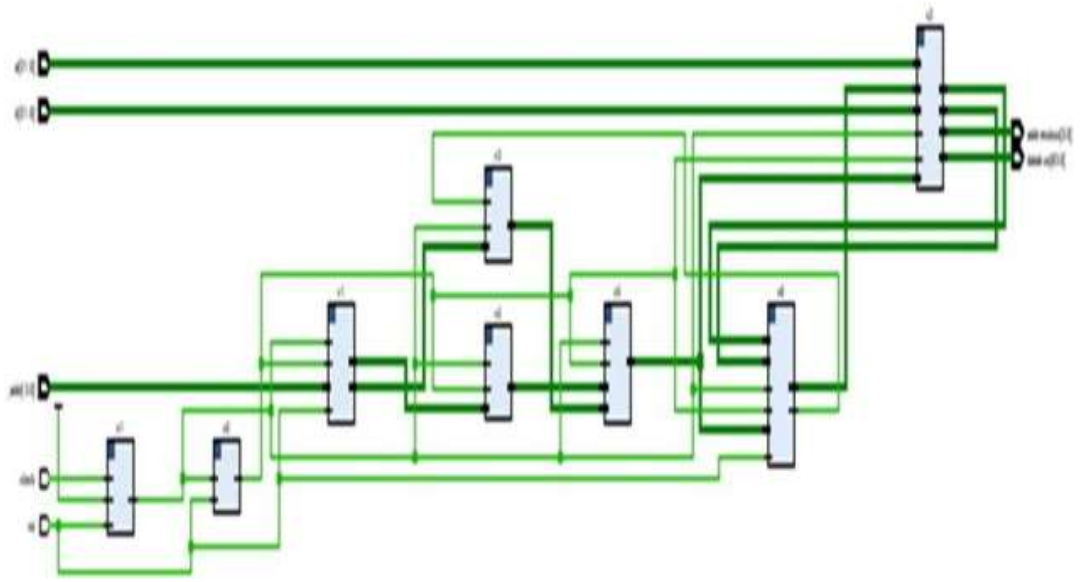
Delay:

From	To	Total Delay	Logic Delay	Net Delay
v2/R0_reg[31]/C	v6/aluout_reg[0]/D	106.244	49.125	57.119
v2/R0_reg[31]/C	v6/aluout_reg[1]/D	103.689	47.310	56.379
v2/R0_reg[31]/C	v6/aluout_reg[2]/D	101.463	45.907	55.556
v2/R0_reg[31]/C	v6/aluout_reg[3]/D	98.201	44.485	53.716

Power:

Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	exp
Top-level Entity Name	processor32bit
Family	Cyclone II
Device	EP2C8F256C6
Power Models	Final
Total Thermal Power Dissipation	56.79 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	25.63 mW
I/O Thermal Power Dissipation	31.16 mW

RTL representation:



Representation of Technology:

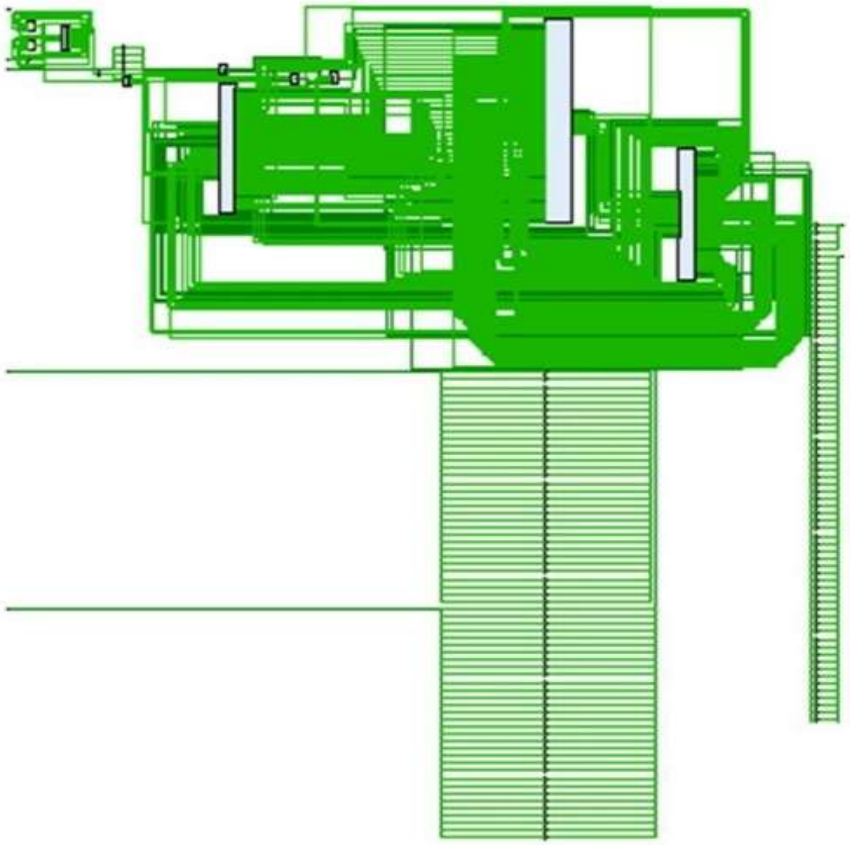


Table 1: Comparison values for time delay & power

	Area in (LUT's)	Time Delay in (ns)	Power in (mW)
Processor32	**3789**	**113.611**	**83.17**
Extension32	**3325**	**106.244**	**56.79**

IV CONCLUSION

In the course of this endeavor, we successfully engineered a RISC processor with an ALU founded on Vedic sutras. By adopting Vedic multipliers not only for multiplication but also as a substitute for conventional adders, we introduced hybrid adders that streamline hardware complexity and markedly enhance area efficiency. This strategic shift not only bolsters performance but also effectively curtails the dimensions and power requirements of multipliers. Moving ahead, our focus extends to implementing MFA (Multiply and Accumulate) functionalities along with a programmable clock mechanism, expanding the application scope beyond that of divide and conquer-based adder optimization, which is not viable for the 32-bit configuration.

Central to this study is the development of a comprehensive Vedic processor amalgamating a Vedic MAC and ALU alongside customary processor components. An intricate set of 14 directives using register addressing modes has been meticulously structured, facilitated by an instruction register and a dedicated 1-bit Z flag register that monitors the ongoing state of mathematical group directives.

Through rigorous simulations, we've meticulously compared the performance of the newly devised Vedic ALU and MAC design against that of the prevailing ALU and MAC setups.

Our innovation doesn't solely pertain to multiplication operations but extends to various other additional operations within the ALU, thanks to the incorporation of mixed adders.
The 32-bit Vedic processor stands out for its trifecta of advantages: a marked reduction in power consumption, a smaller footprint, and diminished latency when compared to conventional processors. The confluence of enhanced performance, reduced power demands, and optimized space utilization stands as the hallmark of this pioneering RISC CPU.

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