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A HIGH-PERFORMANCE FPGA-BASED MULTICROSSBAR PRIORITIZED NETWORK-ON-CHIP

T.R Dinesh Kumar[1]], Dr.Antobennat[2], S.Sanjay[3], A.Balaji [4]„ I.Rattan Kumar[5], C.Saravanan[6], M.Rakshan[7]

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Abstract

In recent decades the demands for high performance semiconductor designs has been emerging steadily. In particular the Multi-core platforms are growing in the design of System-on-Chips (SoCs). The large set wire interconnect in these multi core designs decides the overall system performance both in terms of energy efficiency and attainable speed of data transmission. But with the recent advancement in semiconductor industry with advanced transistor scaling the SoC level design includes more number of dedicated functional blocks in which convention FIFO based single cross bar enabled routers increases the power consumption. In many applications the excessive usage of cross bar restricts the applicability of Network on chip due to its power hungry statistical nature with associated complexity overhead. To mitigate these issues related to the existing NOC, in this paper optimal Finite state machine (FSM) controlled Multi cross bar routers are introduced for routing operation. As compared to conventional Routers in the proposed framework the path delay and associated power is significantly reduced and also avoid possible traffic congestions among routers. The performance metrics also includes asynchronous data transmission between IP blocks with least possible latency overhead.

Keywords—***Network on chip (NoC), routing, IP, FIFO, FPGA, Multicore, Crossbar etc.***

trdinesh@velhightech.com [1],], drmantobenet@veltech.edu.in [2], sanjaysubramanimps@gmail.com [3], balasg2000@gmail.com [4], vh11022_ece20@velhightech.com [5], vh10962_ece20@velhightech.com [6], vh10964_ece20@velhightech.com [7]

[1,2] Assistant Professor, Department of Electronics and Communication Engineering

[3,4,5,6,7]UG Student, Department of Electronics and Communication Engineering

Vel Tech High Tech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai, India.

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I.

II. INTRODUCTION

In recent decades the emergence of system on chip in semiconductor industry and the invention of complex digital system– the power consumption is becoming most challenging than ever and significantly affect both circuit life and reliability. The System-on-Chip (SoC) [1-2] application comes with the integration several Intellectual Property (IP) cores to meet the desired functionality. Inside system component each IP is needs to interconnect with each other for data flow which leads complex wire connections. To accomplish this task network on chip (NoC) is introduced which can replace complex dedicated wire connection by simplified router design. On other side the demands for optimal methodology [3-4] to narrow down power consumption are increasing steadily especially for compact electronic device models such as mobile phone and other 5G related devices. The energy efficiency measures inadequacies inherent in existing NoC models systems have driven the development of new optimal router design for next generation ultralow power applications. In general the overall performance metrics for any NOC system component is largely depends on memory space model [5] used to regulate the traffic flow.

This multi crossbar NoC framework is organized as follows. Section II includes the detailed analyzes of exiting NoC routing models and router design techniques and various energy level optimization models used in different SoC system and its FPGA hardware implementation. Section III discussed proposed Multi crossbar architecture and associated power reduction techniques which includes optimal high performance data flow techniques Section IV summarize the comparative analyzes of proposed crossbar NOC with existing NOC models through FPGA hardware synthesis. Section IV concludes the details.

Counters are the practical system where flip-flops are utilized the most frequently. In microprocessors, they are employed as program counters (PCs), for accessing sequential locations in memory (like ROMs), and for monitoring test progress.

Processing elements (PEs) are components inside high-density developing SoC architectures that interact heavily on-chip and have a major impact on a variety of performance metrics. Due to their high latency, high power consumption, and/or difficult synchronisation, point-to-point and bus-based connectivity do not provide effective on-chip network infrastructures for large SoCs. NoCs are high-performance architectures that were developed to get around the drawbacks of conventional on-chip designs. 1–5 NoCs offer scalable, modular, high-performance connectivity. Moreover, by separating communication and computing units, NoC architectures reduce system complexity.

A NoC has cables, routers, and network interfaces to set up the necessary network infrastructure for connecting PEs. Physical channels make up links of NoCs. Because to their programmability, reconfigurability, rigid internal logic blocks, and abundant routing resources, FPGA devices need a lot of power. NoC structures often offer high-performance and energy-efficient on-chip connectivity while having the potential to benefit from the modularity and reconfigurability of FPGAs. It's vital to note that FPGAs don't employ power-saving measures.

It is always a good idea to physically inspect the circuit before performing any electrical testing because many defects are caused by mechanical issues that are easy to spot, such broken components or poor soldering. Electrical fault-finding techniques are only required in cases where a defective circuit has no visible visual

flaws.Applying every possible input combination and comparing the circuit response to the truth table of the circuit or to the response of a known faultless version of the circuit is a straightforward technique to find defects in circuits that use combinational logic.

There are obvious drawbacks to this approach because, for a combinational circuit, the number of tests required grows exponentially with the number of inputs (n) and equals For a sequential circuit where the sequence of the applied inputs is important, potentially many more tests than this would be required.The ability to access the design's technical specifics at this time is highly desirable.

Finding an elusive defect is made much more challenging and may even be uneconomical if these facts are not available right away. Thus, attempting to gather these technical facts is typically a first duty.So, unless their designers employ strategies at the algorithmic, systemic, and circuit levels to reduce power consumption, FPGA-based designs consume a lot of energy. Several studies 18–30 have focused on analysing and lowering the power consumption of FPGA-based NoCs. It is clear that a NoC built on an FPGA consumes power dynamically to a degree of 78% to 85%.

Because of how well-synchronized with the clock their output signals are, Moore machines are tremendously helpful. The Moore Machine's output signals won't change until the rising edge of the subsequent clock cycle, regardless of when input signals arrive at it. To avoid setup timing violations, this is crucial. One or more of a Mealy machine's outputs and next state signals, for instance, may change at a later time if one or more of its input signals change at some point during a clock cycle. After the setup time threshold for the subsequent rising edge, "some time later" could appear. In this case, the registers holding the FSM's subsequent state can get junk or plain wrong inputs. This clearly indicates that your FSM has a bug or bugs.

III. RELATED WORKS

In this section includes the advantages of existing router design models core and its implications on energy efficiency and reliability measures in detailed. In general both buffered [6] and bufferless [7] router design comes with its own advantages and associated performance constrains. In most cases performance trade-off is unavoidable among these two router design models. Implementation of bufferless router core is applicable only with some energy level optimization models due to its parametric constraints [8].

Very large-scale integration (VLSI) technology advancements in recent years have made it possible to combine thousands of processing components onto a single silicon microchip. MPSoCs, or multiprocessor systems on chips, are the most recent product of this technological development. Network-on-Chip (NoC) has become a scalable and promising connectivity network for MPSoCs to attain high performance.

A routing algorithm is a crucial component of a router in NoCs and gives a packet a path to its destination. Any routing method ought to have two features. Initially, the route selection function needs to be sufficiently adaptable to prevent network sluggishness. Second, it shouldn't provide the surrounding routers with outdated information about the status of network congestion. Several researchers have examined network congestion and suggested methods to reduce/avoid it. These congestion avoidance-based techniques greatly enhance the performance of the NoC. However, they could result in additional hardware costs when side networks are implemented to gather

In [9] introduced lightweight authenticated routing mechanism by detecting the malicious IPs during data communication between routers. Here the

overall system performance SoC by suppressing the DoC attack and avoids successive retransmission of data to the malicious IPs. Experimental observation showed significant improvement in both operating speed and power consumption with least computational complexity overhead. In [10] developed real-time DoS attack by localizing the malicious IP and detecting the successive retransmission measure. Here based on associated latency information computed at each router the validation of the data is evaluated to secure the NoC.high performance dwt transform design.

In [11] introduced energy efficient optimal scheduled deflections for bufferless NoCs. Here time-multiplexing strategy is used for each path links to maximize the network lifetime and offered reliable network operation. Results proved that scheduled NoC increased the life of the network by 62.5%–71.8% with 4%–15% compromise in network performance as compared to existing deflection routing. In [12] investigates the various performance constrains in both buffered and bufferless reconfigurable NoC over XY routing algorithm. Here switching speed and Flexibility in selecting the direction for each port request are compared and deadlock is measured with 3x3 and 4x4 NOC router configuration. Finally performance metrics are analyzed which includes power, transmission latency and attainable data rate. In [13] proposed asymmetrical routing model for 3C NoC architecture using interleaved vertical edge routing algorithm. Here to maximize the system performance novel flit prioritization unit is introduced for bufferless mesh NoC. The results proved that the edge routing measure increased the system performance with least complexity overhead.

IV. MULTI CROSS BAR NOC ARCHITECTURE

In general Cross bar based router NOC additional control signals are transmitted along with along with data input. One control signal transmits in data flow direction which can explore the data input validity and input data availability. Another control signal is transmitted in the opposite direction to stop the flow of data to carry the port availability of each router. This ready signal is used to avoid the data congestion and regulate the traffic flow. In proposed NOC router structures is differ from conventional NOC router with EB buffer and FSM implementation. As compared to FIFO based.

Packets are broken into little, equal-sized flits for wormhole switching (flow control digit or flow control unit). A packet's first flit is routed in a manner similar to that of packets in virtual cut-through routing. After the first flit, the route is set aside for the packet's subsequent flits. Wormhole is the name of this route. Because only one flit needs to be stored at a time in wormhole mode, less memory is needed than in the other two forms. Moreover, there is less delay and a greater chance of a deadlock. By multiplexing several virtual ports to a single physical port, the danger of traffic congestion and blocking can be mitigated. As non-local information may make the design more difficult, the router's local information is taken into account.VC channel EB channel reduces the payload latency significantly while preserving functionality of NOC. Here packet is also includes Header portion with four bit size called Flit which includes the destination address which is used for NOC port routing. In accordance with number of routers used in NOC the flit size is configured to accommodate the source and destination address. Journal of Scientific Research in Science, Technology, and Engineering.

The other two modules are in charge of controlling the data-path with message transmission. The data-path is a vital component of message storing. The following definitions describe two writing and reading processes. The write is

specified from the perspective of the transfer initiator, and the message data should be saved in the mailbox prior to the initiator starting the transfer. In other words, initiators own the mailbox and have complete authority to compose their mails. After one initiator has stored the messages in the mailbox's data-path, the mailbox is not enabled until the initiator sends, and this is designated as the read.

FSM based buffer flow control

Here FSM based buffer flow control is used to reduce the FIFO size associated to each virtual channel (VC). By incorporating buffer inside router design data flow between router is regulated which can avoid data congestion and reduce the data overhead in FIFO channel. In Elastic buffer channel two different inputs are gated with two independent master- slave flip flops. In proposed NOC architecture, only buffer channels are used for data buffering instead of conventional FIFO based virtual channel. With controlled data flow and associated traffic rate the FIFO size significantly reduce. The NOC network with elastic buffer channel offers significant energy efficiency and improved throughput rate with reduced packet latency. When the left switch is hit, the FSM should transition to the BACKUP RIGHT state, and when the right switch is pressed, it should transition to the BACKUP LEFT state.

The next ones are a little distinct. We want them to just flow to the following state, but we can't allow them to do so instantly because then the robot won't have time to back up or turn! It will seem like nothing happened since it will happen so quickly. We must add a counter to maintain the state for a longer period of time.As a counter needs some flip-flops to store its value, it cannot be a component of the FSM.

Many practical methods for describing systems at a high level of abstraction are discussed in this chapter. This chapter discusses the methods by which we can effectively consider complex systems at a very high level of abstraction, whether this be for digital systems using finite state machines or algorithmic state machines, or for more abstract systems utilizing Laplace or Z domain techniques. Examples are given to show how the use of a "block level" technique in the context of graphical modeling might aid in the comprehension and application of models at this level.

The most frequent kind of software vulnerabilities have been buffer overflow flaws. The detection of potential program vulnerabilities takes a lot of time and effort. This article suggests a finite state machine-based analysis model of buffer overflow vulnerability (FSM). The model analyzes source code statically. The process of data overflow and the development of buffer overflow vulnerabilities are next examined. The corresponding vulnerability analysis model is created for the two categories of buffer overflow vulnerabilities brought on by function call errors and loop copy problems. Two scenarios are used to validate the vulnerability analysis approach that is described in this study. The experimental findings demonstrate that the model is capable of quickly and accurately identifying buffer overflow vulnerabilities.The internal router functionalities employed in Network on Chip (NoC) infrastructure present various obstacles for the creation of efficient architectures for communication in on chip multiprocessor systems. The on-chip router should be created to offer improved granularity in per-flit processing. In fact, the ability of the router to prevent congestion and provide effective data-flow control determines the quality of service experienced at the application level. As a result, an improved router architecture is required to deliver the desired QoS.

In order to provide flow-control mechanisms for congestion avoidance while taking quality of service into account,

this study offers an internal router architecture for on-chip communication. It explains the router's internal operations for the best output flit scheduling as well as its capacity to implement per-class service for incoming flows.

The paper's primary focus is on the description and performance evaluation of two data flow control proposals that can be employed with the suggested router design. The findings of this study demonstrate that implementing these suggested strategies in NoC leads in an intriguing improvement in the measured end-to-end QoS. To demonstrate that the suggested solution outperforms previous schemes and maintains an intriguing trade-off with hardware characteristics when created using 45 nm integration technology, we thoroughly compared the offered solutions with those already existing schemes published in the literature.

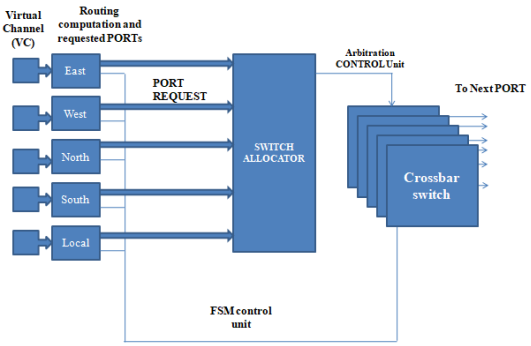

Figure 1 Proposed multi cross bar NoC architecture

Multi cross bar switch design

The basic computations involved in proposed multi cross bar NOC includes VC FIFO channel model for each port inputs (N,E,W,N,S),Switch allocator, and FSM based data flow control unit for most simplified data flow operation for NoC routing. To maximize the performance speed NoC speed of routing convergence multi crossbar switch is introduced which is also optimized the associated switching activities which is not uniform in other existing NoC architecture across different design models. But energy and performance efficiency is achieved with notable computational complexity trade-off with the inclusion of several crossbar switches.

For the most part, digital design is based on finite state machines (FSMs). The fundamental function of an FSM is to store a sequence of distinct states and transition between them in accordance with the values of the inputs and the machine's current state. There are two different forms of FSM: Moore (where the state machine's output is solely based on the state variables) and Mealy (where the output can depend on the current state variable values AND the input values).

the functional layout of a crossbar switch coupled to a single memory module. For communication with the memory module, the circuit incorporates multiplexers that choose the data, address, and control from one CPU. When two or more CPUs attempt to access the same memory at the same time, arbitration logic established priority levels to choose one CPU. The priority encoder in the arbitration circuitry generates binary code that can be processed by the multiplexers.

Many cross points are maintained at junctions where the pathways of the memory module and processor buses cross in the Crossbar Switch system. The little square at each cross point is a switch that determines the route from a CPU to a memory module. In order to configure the transfer channel between a memory and a processor, each switch point has control logic. It determines whether the address for its specific module on the bus has been calculated. Also, on the basis of a defined priority, it rejects numerous requests for access to the same memory module.

Flow-control techniques can be categorized according to how precisely channel bandwidth and buffer allocation are handled [9]. A flit is the fundamental unit of bandwidth and storage allocation

(flow control digit). Sequences of flits are used to segment packets. Flits don't contain routing or sequencing information, unlike packets. The bandwidth and buffer allocation method known as flit-buffer flow control uses flits. This has three benefits: (a) it minimizes the amount of storage needed for a router to operate properly; (b) it offers stiffer backpressure from a point of congestion back to the source of a flux stream; and (c) it makes storage more effectively utilised. Due to the fact that these benefits complement on-chip communication's features nicely,

V. EXPERIMENTAL RESULTS

In this section, the performance metrics of proposed elastic buffer enabled NOC over conventional FIFO based NOC model and validated the metrics both in terms payload rate and switching activity control with associated energy efficiency measures. As compared FIFO based data flow control the proposed elastic buffer based VC channels showed significant memory space reduction and power consumption rate with least possible hardware complexity overhead. The proposed NOC core is modeled using the Verilog HDL and synthesized using INTEL QUARTUS II FPGA synthesizer for comparative analyzes as shown in Figure 2. The elastic buffer channel in NOC router offered flexible memory space tradeoff and tolerable error protection due to its controlled data flow.

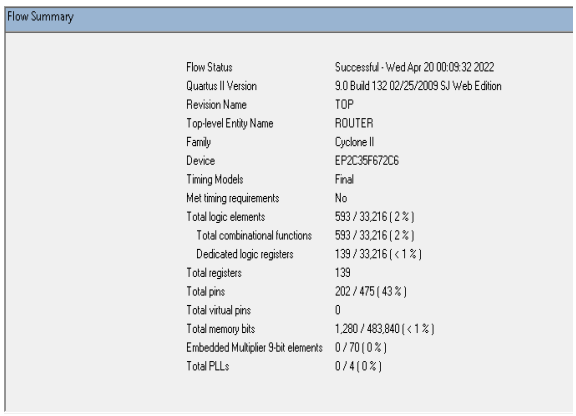

Figure 2 Hardware report summary

Signal transition reduction efficiency

In general the computations involved in FIFO based router unit are highly complex which leads more signal transitions and associated power consumption as shown in table 3.2 since large number of memory units are involved, resulting at each virtual channel with maximum signal transitions. Though several optimization models support high speed and complexity reduction, problem arises in terms of signal transitions. Here in this framework only minimum number iterations are involved in each router stage which can minimize the overall transition rates.The functional level net lists are generated using vector waveform file (.vwf file) from post simulations. Transition simulator tool is used to compute the dynamic signal transitions as shown in Figure 3 and Figure 4.

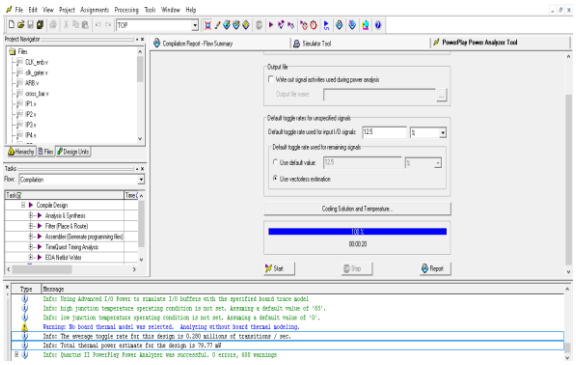

Figure 3 Signal transition report

Table 1 Energy efficiency and switching activity performance comparisons

NOC model	Number of transitions (millions/sec)	Total power consumption (mW)
Existing NOC	37.56	372.65mW
Proposed multi crossbar NOC	25.581	269.09mW

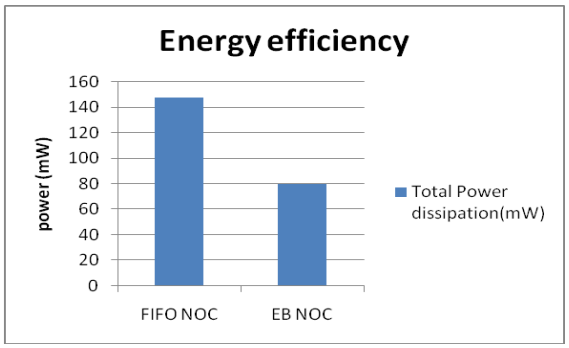

Figure 4 Energy Efficiency Performance Comparisons

The efficiency of power optimization through data transition reduction scheme is analyzed using dynamic power management (DPM) in terms of both digital transition reduction and associated dynamic power consumption reduction as shown in table 2. To illustrate the energy efficiency during the evaluation of signal constellation post simulation has been carried out which will generate the value change dump (.vcd) file. The dynamic digital transitions during iterative computation and associated switching activities are note down for energy measurements. The power play power analyzer tool is used to compute the overall power dissipation which includes both static and dynamic power as shown in table 1

Table 2 Performance comparisons between proposed multi cross bar NoC vs. existing NoC using FPGA hardware synthesis results

NOC model	Area(LE's used)	Fmax (MHz)
Existing NOC	562	206.27 MHz
Proposed multi crossbar NOC	593	816.99 MHz

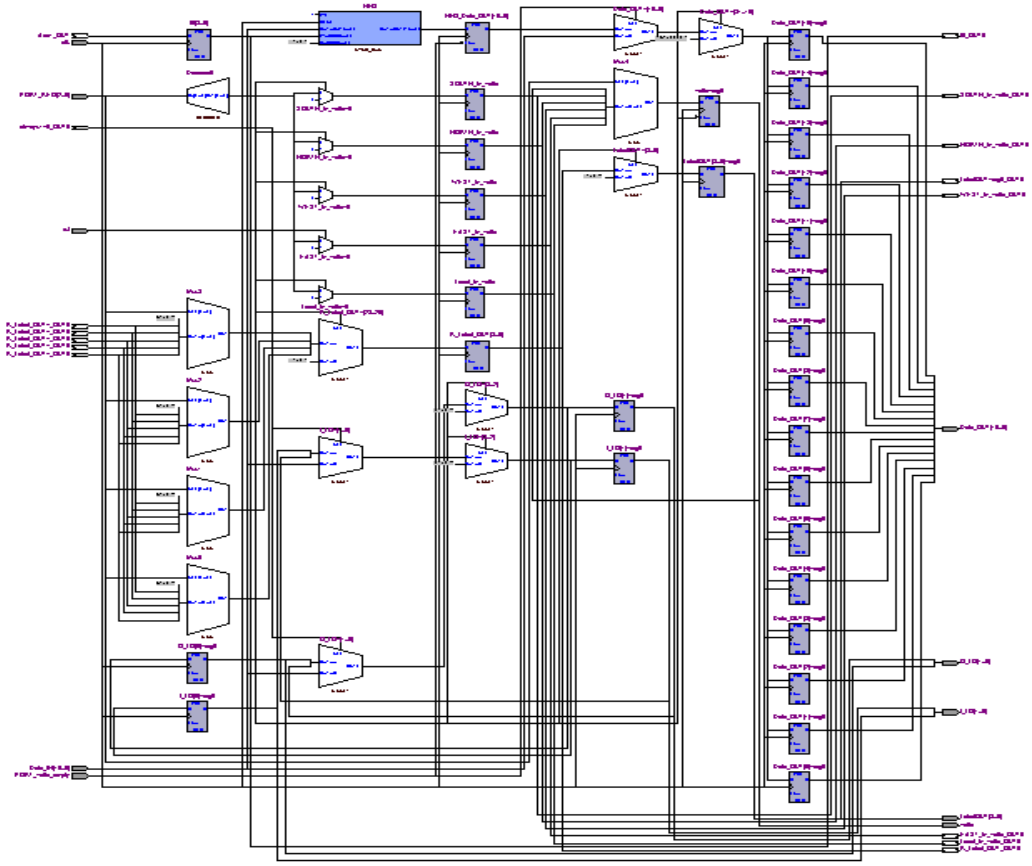

Figure 5 RTL schematic view

VI. CONCLUSION

Here in this paper high performance multi cross based NoC architecture is presented for optimal router implementation for next generation complex SoC designs with improved performance measures. Here FSM based elastic buffer channel is used and evaluated as NoC information link to regulate the data flow. Here, in proposed memory efficient NOC router architecture Elastic buffer channel is used as VC data buffering as potential replacement to FIFO, which comprise of only two registers and one FSM controller to assert control signals. By merging this optimal multi cross operation and associated NoC data buffering path delay is significantly reduced. From the experimental results it is well proved that the proposed path delay optimized Multi crossbar router based NoC design offered improved performance efficiency as compared to convention NoC model. High-density integrated circuits utilising field programmable gate arrays (FPGAs) for quick prototyping and reconfigurable digital circuits have been made possible by high performance system-on-chip (SoC) designs. A network-on-chip (NoC) that can be customised for a variety of uses can be designed using FPGA configurability. For the implementation of extremely large SoCs, NoC designs offer effective communication infrastructures. In this paper, we suggest HiFMP, a high-performance multicrossbar prioritised NoC router built on FPGA technology. The suggested router's goal is to develop a low-power NoC router with excellent energy-efficiency, network throughput, area, and latency performance for effective FPGA realization. HiFMP is a parameterizable router that works well with a mesh topology in an FPGA-based NoC. Network-level analysis and hardware exploration are included in performance evaluations; the outcomes show the efficacy and high performance.

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