Efficient VLSI-Architecture of FIR-Filter for processingSeismic-Signal

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Abstract – The main requirements for filters used in real-time seismic warning systems are low complexity, high speed, and reconfigurability. To achieve these objectives, a combination of techniques is employed. This includes minimizing logic operators and logic depths within the FIR filter and using a Carry Look Ahead Adder (CLA) to reduce critical path delay (CPD). Additionally, the common sub-expression elimination (CSE) technique, based on canonical signed digits (CSD), is commonly utilized to decrease hardware complexity. The proposed design of an efficient FIR filter incorporates the techniques. This results in several advantages, including superior performance in terms of area, power, and delay. The implementation of this architecture is done using Verilog, and the results obtained are analyzed through simulation utilizing Xilinx Vivado 2019.1 and Cadence 45nm technology. The architecture proposed yields a 3%,70%, and 83% reduction in CPD, Number of LUTs, and SDP over state of art CSE-based architecture.

Index Terms—Finite impulse response (FIR), a canonical signed digit (CSD), common sub-expression elimination (CSE), carry look-ahead adder (CLA), Vertical Common Sub Expression (VCSE), Horizontal Common Sub Expression(HCSE), Partial Product(PP).

I. INTRODUCTION

Seismic refers to an earthquake or something related to one. Sometimes noise may be added to this signal and it will be difficult for the alert system of Seismic to recognize whether the signal is due to an earthquake, volcano, etc; The key problem in processing the seismic signal is to remove the noise, which can occasionally be added to the signal. For calculation, band selection, signal analysis, etc., digital filters are utilized. Finite Impulse Response Filter is the name given to the impulse response over a finite time period. Many of its uses are in the areas of image processing, voice processing, and signal processing for signals in signals. The FIR filter is important in creating effective stable filters with linear phase and unconditional stability because of its outstanding properties. The main goal of this filter is to maintain important signals by clipping off undesired noise and distortion. This filter is beneficial for significant signal processing applications because of the critical components such as pre-processing of signal, anti-aliasing, band selection, interpolation, and low-pass filtering. The FIR filter will emerge as the best option because it does not require bit truncation or bit rounding to produce a noise-free filter. Low complexity, high speed, and reconfigurability are the three main demands of these FIR filters which are used in the processing of the obtained seismic signal in a real-time alert system of Seismic. Realizing these filters with the appropriate accuracy level in real time is a difficult undertaking. Many techniques and methods have been realized in existing [10]-[15] in designing efficient FIR filters.

The optimized FIR filter is done by using CSE (Common Sub Expression Elimination Method) and has gained more importance in reference papers [1]-[7], and the use of adders like CLA [8][9]. Therefore the main aim is to design an efficient VLSI architecture for FIR filter.

The major works which are done are presented in this brief are as follows.

i) The pre-processing of seismic signals has been implemented using a high-speed and low-power FIR filter. The suggested architecture employs the CSE algorithm with CSD-coded filter coefficients as input data to reduce hardware costs. Carry Look Ahead Adder (CLA) is also used to attain high speed (low CPD). The proposed structure outperforms the FIR architectures already in use, according to a comparison of FIR filter architecture for seismic applications [1].

ii) The crucial requirement for real-time applications is the dynamically changeable filter coefficients. Consequently, the state-of-the-art[1] in terms of complexity of hardware and CPD is outperformed by the CSE-based architecture that has been presented. The outline of the brief is as follows.

The current algorithms are discussed in Section II. Section III of the approach has been made available. Section IV discusses the FIR filter's potential VLSI architectures. Results obtained from the implementation are provided in Section V. Section VI brings the brief to a close.

II. PRELIMINARIES

In a structure where a group of constant multipliers is used for multiplying a common variable, such as when the common input x(n) variable is multiplied with all the constant coefficients H(n), using fundamental operations like addition, and hardware shifting to get the output, the CSE (Common Sub Expression Elimination) algorithm technique is used to minimize the logical operators and logical depths to reduce the hardware complexity.

1) ***Encoding Coefficients of Filter in CSD:*** To reduce the hardware expense of the FIR design, constant coefficients might be represented as canonical signed digits (CSD). CSD can represent a signed number with bit values -1,0,1. For example, Consider the 4-bit representation in binary of decimal value ho= 7, i.e., 0111, then the CSD representation of 7 can be written as (2^(3)-2^(0)) and in binary representation (100-1). As there are three nonzero bits, constant multiplication requires the use of two adders. However, the 4-bit CSD representation will be 100-1, contain only two non-zero bits, and multiply (ho X x(n)) with a single adder/subtractor operation.
Generating Magnitude and Sign values of each coefficient for their respective CSD values that is the above CSD coefficient value will have a Sign value of h0=0001 and a Magnitude value of h0=1001.

2) ***CSD-Based VCSE (Vertical CSE) Algorithm:*** There is a presence of vertical common sub-expressions (VCSs) i.e,[1 1] and [1 $\bar{1}$] and their versions of negative vertically[1][2][3] in CSD-based coefficients of a filter as shown in Fig.3.

3) ***CSD-Based HCSE (Vertical CSE) Algorithm:*** We can also observe there is a repetitive occurrence of HCSs [101], [10$\bar{1}$], [1001], [100$\bar{1}$] and their versions of negative in CSD-based filter coefficients [1][2][3] as shown in Fig.3.

4) ***CLA (Carry Look-Ahead Adder):*** The adder produces carry propagation delay while performing other arithmetic operations like multiplication and divisions as it uses several addition or subtraction steps. This is a major problem for the adder and hence improving the speed of addition will improve the speed of all other arithmetic operations. Hence reducing the carry propagation delay of adders is of great importance. There are different logic design approaches that have been employed to overcome the carry propagation problem. One widely used approach is to employ a carry look-ahead which solves the delay problem by calculating the carry in advance, based on the inputs [8][9].

III. METHODOLOGY

The flow chart of the methodology of the Filter proposed is shown in Fig.1 and the steps are described below.

i)Generating the coefficients of desired frequency fromMatlab based on the order numbers.
ii) Getting the CSD representation of filter coefficients and storing their sign and magnitude values in LUTs as in Fig.3.
iii) Sign and magnitude bit is partitioned into 5 groups of 3bits P1=(s[14:12], m[14:12]), P2=(s[11:9],m[11:9]), P3=(s[8:6],m[8:6]),P4=(s[5:3],m[5:3]), P5=(s[2:0],m[2:0]).
iv) Partial product unit to generate the products partially by add and shift technique.
v) 3-bit CSDs used are "001", "010", "100", "101", and "10$\bar{1}$" and their versions of negative, which produce partial products(x1-x10).
vi) Control Signal Generator identifies similarity among partitioned groups by comparing sign and magnitude parts of every group with others and reducing the logical operators is done.
vii) Based on 3-bit VHCSE, partial products are chosen using muxes.
viii) Area, power, and latency are reduced by CLA.[8][9].
ix)Synthesis is done in both Xilinx Vivado 2019.1 and Cadence 45nm technology to obtain area, power, and delay.

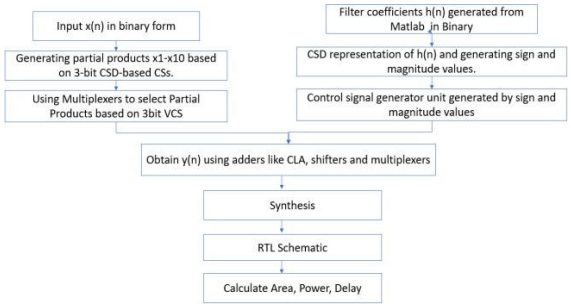


Fig. 1. Proposed Methodology Flow Chart

IV. VLSI ARCHITECTURE OF PROPOSED FIR FILTER

Proposed Filter Architecture:

The four units make up the proposed FIR filter's architecture (i) A unit for generating partial products (PPs) using the shift-and-add method. The CSG compares the magnitude and sign components of every group with those of the other groups to determine if groups P1 to P5 are comparable to one another. The inside structure of PP generating (PPG) is seen in Fig.4. Fig.6 depicts the internal organization of the control signal unit; (iii) Muxes (MUX2- MUX6) layer selects the PP according to 3-bit VHCSE as illustrated in Fig.5. (iv) an added layer under control according to the CSE, Carry Look Ahead adders are utilized to carry the controlled additions of multiplexers (MUX7-MUX16) PPs. CPD is decreased with CLA adder. [8][9].

The main blocks of FIR Filter architecture include

1) CSD, Sign, and Magnitude values format:

Fig.3 shows an example of the CSD representation of 3rd-order 16-bit coefficients for certain frequencies and their sign and magnitude representation values and how they will be stored in LUTs [2].

CSD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H0	0	0	-1	0	0	-1	0	1	0	0	0	-1	0	1	0	0
H1	0	1	0	-1	0	0	-1	0	1	0	1	0	1	0	0	0
H2	1	0	1	0	1	0	-1	0	1	0	0	1	0	-1	0	0
H3	1	0	1	0	1	0	0	-1	0	1	0	-1	0	0	0	-1

Magnitude

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H0	0	0	1	0	0	1	0	1	0	0	0	1	0	1	0	0
H1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	0
H2	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0
H3	1	0	1	0	1	0	0	1	0	1	0	1	0	0	0	1

Sign

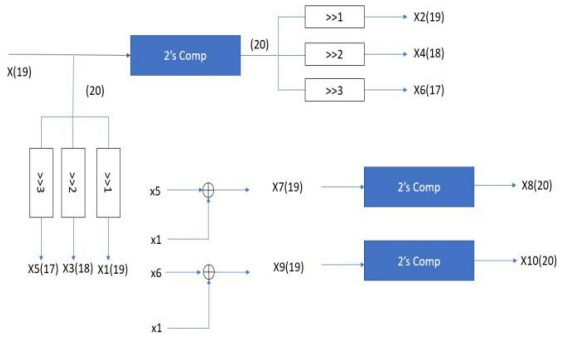
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
H1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
H2	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
H3	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Fig. 2. CSD VHCSE algorithm applied on coefficient set of 3-tap filter

2) Partial Product Generator:

The partial product generator unit Fig.3 is obtained from the Fig.5 which doesn't contains a consequent number of one's according to the CSE algorithm. Considering the 3-bit representation of our CSD values, the possible repetitive patterns x1 to x10 are generated. Where x1, x3, x5, x7, x9 and their negative versions x2, x4, x6, x8, x10 are obtained by 2's complement.

Fig. 3. Partial Product Generator



H[2]	H[1]	H[0]	M[2]	M[1]	M[0]	S[2]	S[1]	S[0]	N0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0	x1
0	0	-1	0	0	1	0	0	1	x2
0	1	0	0	1	0	0	0	0	x3
0	-1	0	0	1	0	0	1	0	x4
1	0	0	1	0	0	0	0	0	x5
-1	0	0	1	0	0	1	0	0	x6
1	0	1	1	0	1	0	0	0	x7
1	0	-1	1	0	1	0	1	0	x9

x7 = x1 + x5 = 101
X8=2'scomp(x7)

X9 = x1 + x6=10 $\bar{1}$
X10= 2's comp(x9)

Fig. 4. Partial Product Generator for 3-bit CSD-Based Common Sub Expressions.

3) Control Signal Generator:

Control Signal Generator Unit takes the 16-bit coefficients generated from Matlab and partitions the Sign and magnitude bits of CSD-based coefficients into 5 groups of 3bits P1=(s[14:12], m[14:12]), P2=(s[11:9],m[11:9]), P3=(s[8:6],m[8:6]), P4=(s[5:3],m[5:3]), P5=(s[2:0],m[2:0]). The Control Signal Generator block will produce 10 control signals depending on the equality check for 10 different cases. The control signal generator unit is seen in Fig.5. It compares the sign and magnitude components of each partitioned group with those of the other groups to determine how similar they are.

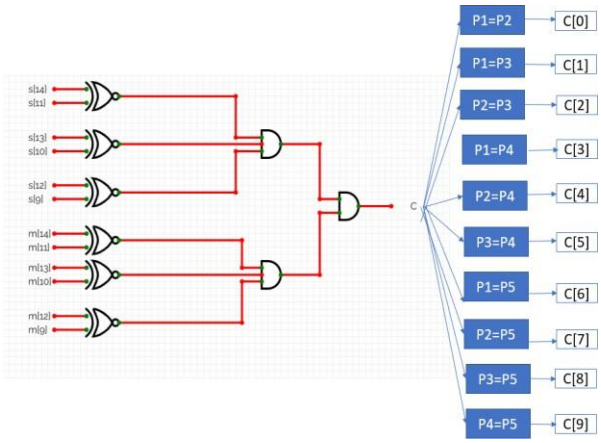


Fig. 5. Control Signal Generator Unit1

4) MUX2-MUX6:

The mux layer selects partial product corresponding to 3bit CSE as in Fig.2.

5) MUX7-MUX16:

These muxes select partitioned groups, where P1 is compared with P2, if P1 is the same as that of P2 then it is right shifted

by 3 bits, again p1 is compared with P3, if it is the same then it is right shifted by 6 bits and so on.
Similarly, P2 is compared with P3, P4, and P5 and they are shifted based on the comparison.
And this continues with the other groups P3, P4, and P5 .

V. ASIC AND FPGA IMPLEMENTATION RESULTS AND COMPARISON

The behavioral model of the filter is coded in Verilog. By Xilinx's Vivado design suite 2019.1, we were able to synthesize the filter while optimizing the design. As the target device, we used the Xilinx ZYNQ-XC7Z020-1CLG484 FPGA device, and we got results from the synthesis and implementation. Cadence's 45nm technology library has been used to develop ASICs. The proposed architecture and the current architecture [1] have been compared, as shown in Table 2.

FPGA IMPLEMENTATION(ZYNQ-XC7Z020):

1) RTL SCHEMATIC CIRCUIT:

After the synthesis and optimization processes, this schematic circuit Fig 6. is produced. It displays how the design is represented in terms of logic elements that have been optimized to the particular Xilinx device or "technology"; for example, in terms of LUTs, carry logic, I/O buffers, and other components.

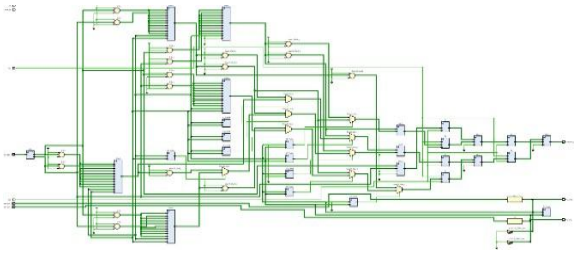


Fig. 6. RTL Schematic Circuit of FIR Filter Proposed Architecture

2) RTL TECHNOLOGY SCHEMATIC:

After the synthesis process optimization and technology targeting phase, this schematic Fig. is produced.

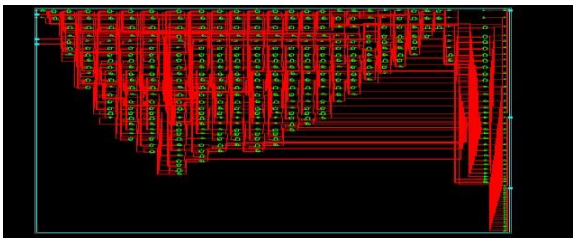


Fig. 7. Technology Schematic of FIR Filter Proposed Architecture

3) LUTs:

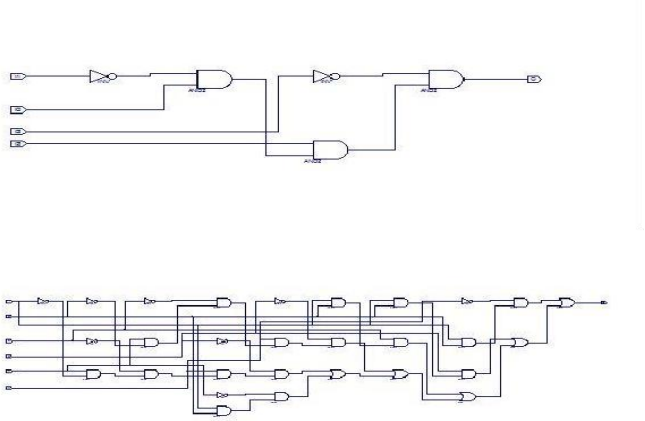


Fig. 8. LUTs of FIR Filter Proposed Architecture

Fig.8 shows the LUTs of the proposed filter. The LUT is the basic building block of an FPGA and is capable of implementing any logic function of N Boolean variables. Essentially, this acts as a truth table in which different combinations of the inputs implement different functions to yield output values.

TABLE I

VLSI FPGA IMPLEMENTATION FOR PROPOSED ARCHITECTURE

Filter Order	NOS	SLUT	Slice Registers	Power	CPD(ns)	SDP(us)
CLA(16)	60	190	100	0.131	2.811	0.168
CLA(20)	76	231	100	0.130	2.897	0.220

CLA-Carry Look-Ahead Adder

NOS- Number of Slices
SLUT- Slice LUT
CPD-Critical Path Delay
SDP-Slice Delay Product

Table I shows the results of area, power, and CPD of s16th and 20th orders of the Filter architecture proposed. The Slice numbers in the 16th Order and 20th Order are 30 and 33, the Slice numbers LUTs are 176 and 211 in the 16th and 20th Order, and the Slice numbers Registersares 98 and 100 in the 16th and 20th Order. Power Dessiptaed in the 16th and 20th Order is 0.131W and 0.130 W. The Critical path delay(CPD) of the 16th and 20th Orders is 2.67ns and 2.96ns, and the SDP is 0.080(us) and 0.097(us) for the 16th and 20th Orders.

4) CRITICAL PATH DELAY OF 16TH ORDER FILTER USING CLA:

The CPD of the 16th order in our FIR filter Proposed is 2.811ns from R0/Out_Reg[1]/C to R4 /Out_Reg[17]/D as shown in Fig.9.

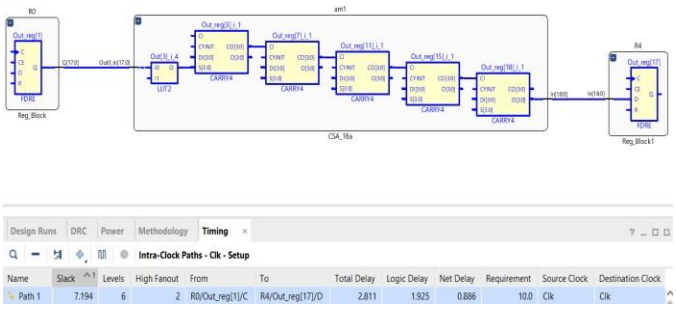


Fig. 9. CPD of CLA 16th Order

TABLE II

VLSI FPGA IMPLEMENTATION COMPARISON

Filter Order	Number of SLUT's	CPD(ns)	SDP(us)
Order 16th Existing[1]	746	2.88	1.298
Order 16th Proposed	190	2.811	0.168
Order 20th Existing[1]	771	2.96	1.385
Order 20th Proposed	231	2.897	0.220

CLA: Carry Look Ahead Adder. SLUT: Slice Look-Up-Tables. CPD: Critical-Path-Delay. SDP: Slice-Delay-Product

VI. CONCLUSION

In this work, an FIR Filter architecture is proposed. Matlab tool is used to generate Coefficients of different Orders of different frequencies based on input signal frequency. The FIR filter proposed is coded in Verilog and it was simulated and synthesized using Xilinx Vivado 2019.1 tool. The proposed Filter provides less delay compared with the existing Filter by 3%. Table II represents the area summary of different Filters where the proposed Filter consumes 25%, less area compared with the existing reconfigurable FIR Filter. Table I shows the complete area, power and delay summary of our proposed FIR Filter for the 16th and 20th Orders. Red Hat Enterprise 6 Workstation is used to implement the same FIR Filter Proposed in Cadence 45nm Technology to generate area, power, and delay reports and their schematic. Table III shows the area, power, and delay of the 16th and 20th Orders of the Proposed Filter obtained from Cadence 45nm technology.

VII. FUTURE WORK

The real-time seismic signal can be given as input to the designed digital filter on hardware to observe the filter of noise with good accuracy.

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