STEEPER SLOPE CHARACTERISTICS OF DM FINTFET

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Abstract

As device dimensions are scaled, using strained Channels as functionality booster becomes more special significance. Tunnel field effect transistor (TFET) has to play the most imminent role in the future technology of the transistors. The intent with this paper will be really to do research of Single gate (SG) TFET, Double gate (DG) TFET out of the initial point to prior now. This paper evinced structural models of Double metal FinTFET. The proposed model improving the performance and at same time more concentrated on decrease the limitation of TFET i.e., maintain the steeper slope, improve the drive (I_{ON}) current and reduces ambipolar leakage(I_{OFF}) current. This result develops the subthreshold swing (SS) by 18.2 mV/decade, drive current (I_{ON}) is close to 10^{-6} A/µm, leakage current (I_{OFF}) is close to 10^{-15} A/µm and also diminish the ambipolarity of the device compared to the FinTFET.

Keywords: Tunnel FET, SG-TFET,DG-TFET and TG-TFET, sub-threshold slope(SS), Drive (I_{ON}) current , Ambipolar leakage(I_{OFF}) current.

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1. INTRODUCTION

The traditional devices are overwhelmed with short-channel effects (SCEs) below 45 nm. Ample research is awestruck with the new device such as FinFET, as it has good electrostatic control over the channel [1], thereby controlling a better number of SCEs. More than two decades have passed since the FinFET became the best replacement for planar devices. Nonetheless, with the technology scaled down below 7nm, FinFET performance has plummeted. In non-classical devices, SS value not exceeds 60 mV/dec, so the supply voltage can be lowered [2] is shown in Fig(1). As a result, it played a minor role in the history of technology. It is important to look for new device structures that achieve the physical limit of SS value. A low SS value indicates a high switching frequency, so steeper features are required for high-speed devices. The rapid on/off switching makes it ideal for power-saving uses. Continuous research unveiled a device called TFET as the best replacement for the FinFET device below the 7nm technology.

In the context of sub-threshold slope (SS), low leakage current became the cynosure. The basic working of TFET has a band-to-band tunnelling (BTBT) mechanism. This BTBT mechanism can decrease the off-state (I_{OFF}) current and also break down the physical limit of SS less than 60 mV/decade. There is a high demand for precise devices in sub-7nm technology. A new technique was introduced in the TFET device to improve the on-state current and reduce SCEs.

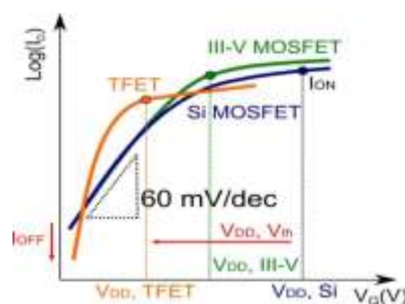

Fig .1 I_d – V_{gs} characteristics of MOS FET and TFET device [4].

WORKING MECHANISUM OF TFET

A p-i-n junction channel design is used in the fundamental building blocks of a TFET [3]. The basic TFET device is illustrated in Fig.2, and it has both a p-type source and an n-type drain. Additionally, it can function with a variety of gate biases. The transistor has a severely doped p+ source, a moderately doped n-type channel, and a heavily doped drain. In most cases, the TFET present will comprise a number of various parameters such as I_{GEN}, I_{BTBT}, and I_s. I_{GEN}, or generation current, is a component of reverse-biased voltage and is determined by the formation of holes and electrons in depletion zones[4]. This process is reliant upon the flow of current through the device. IBTBT, also known as BTBT current, depends on this carrier tunnelling in the filled band of its origin to an open group at the station. A diffusion-induced reverse saturation current is more accurate.

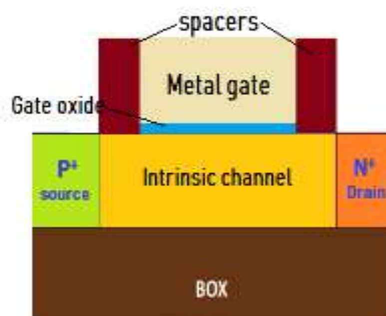

Fig 2. Cross section view of Tunnel FET.

The switching activity of a TFET may be in either the OFF or ON state. Both of these states are possible. The behaviour of the TFET is related to that of a p-i-n diode when there is no field influence coming from the gate, and the tunnel space is big and proportionate to the length of the intrinsic area, as seen in the energy band diagram of Figure 3.

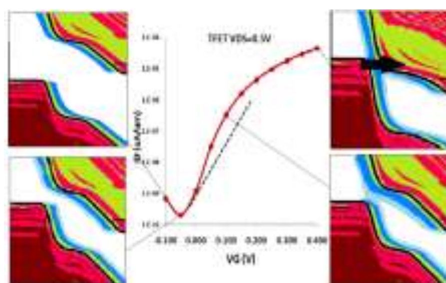

Fig 3.Energy band diagram Tunnel FET in ON and OFF state

BTBT is low, and the TFET is off [5]. I_{OFF}, measured in pA/m, is very low in TFETs and handy for low-power applications. Figure 3 shows the energy band diagram of an ON-state TFET. If the gate bias voltage exceeds the band gap, the valence will connect to the conduction band near the source. Since the tunnel route is shorter than the intrinsic area, BTBT is rising. Gate bias reduces tunnelling distance and increases drain-source current (I_{ON}).

LITERATURE SURVAY

Tunnel FETs often have low driving current (Ion) in comparison to ITRS requirements because of the large BTBT barrier, which is common in semiconductors with wide band gaps such as silicon. Dielectrics with a high-k gate are preferred for high ON current. High-k dielectric gates [6] increase capacitive coupling between the gate and the source-channel tunnel junction, resulting in larger TFET current. Bandgap engineering [7], enhanced hetero structures [8], low bandgap materials, gate to source overlapping technique[9], and channel doping level variation [10] depending on tunnel direction are all important results in this field of study. The majority of the study effort has been disclosed, notably on the enhancement of device gate control over the channel, which will increase the drive current. In this purpose, study the different gate engineering techniques are used to improve the parameters of on state current and subthreshold slope.

Single gate Tunnel FET (SG TFET)

From the perspective of gate orientation, the tunnelling mechanism is divided into point tunnelling as shown in Fig. 4(a) and line tunnelling[11] as shown in Fig. 4(b). The smallest amount of charge carrier BTBT production occurs at the source to channel intersection area, or point tunnelling.

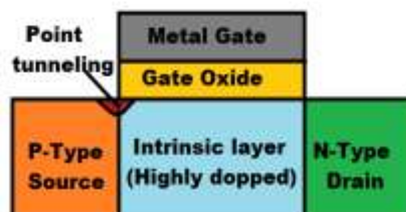

Fig 4.(a) Point tunneling TFET

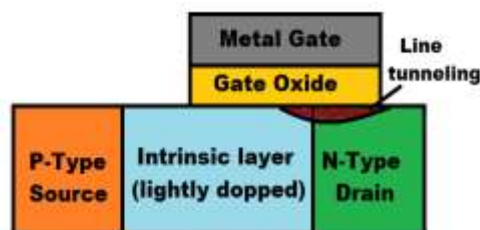

Fig 4.(b) Line tunneling TFET

The gate is presently overlapping the foundation since it was built inside of this equipment, which has an effect on higher rate carriers. Line tunnelling, which occurs in a significant portion of the gate overlap source part to channel junction, is where BTBT production speeds occur. The main advantage will be in LTFET, which will provide more tunnelling current. It was argued that promoting line tunnelling FETs would improve the device's performance. A high-dielectric was utilised as the gate insulator or spacer by Xiangzhan Wang et al.[12] to augment the TFET and enhance its subthreshold properties. A gate field plate TFET (GFP-TFET) construction is suggested in this study to improve driving current and reduce current kink brought on by fringe-induced barrier lowering. Ion/Ioff is 10^{13} and SS=21.4 mv/dec were attained. D. B.Abdi et al.[13] proposed that the Ion-Ioff threshold voltage of TEFETs with dual material gates be significantly increased. Subthreshold slope may also be made better. To bring about the

general betterment Dielectric of high K has been used. Stefan Glass et al [14] stated that a novel technique to reduce the ambipolar effect and improve the I_{ON} current the best design for a hetero-dielectric device is said to be one with a highly doped SiGe pocket at the source-channel junction

Double gate TFET (DG TFET)

Fig.5 depicts the fundamental structure of an n-channel DG TFET. The doping concentration of the P-source, n-drain, and n-type intrinsic station areas is 10^{19} cm-3 and 10^{17} cm^{-3}, correspondingly. The metal gate work function (m) is 4.6 eV utilizing a 3 nm SiO_2 layer and a 7 nm spacer (HfO_2) material thickness. The front gate is normally linked to the device's top side, while the rear gate is often attached to the device's bottom side. Both the I_{ON}/I_{OFF} ratio and the SS improve when there is dual-gate control on two channels through which current can flow at the same time. According to Muhammad Elgamal et al.[15], the most effective way to boost ON current caused by accumulative tunnelling is to reduce the gate dielectric thickness by one, and then use a material containing hafnium dioxide in order to get a large dielectric constant [16]. There are many different gate chemicals that may be employed to improve the ON and OFF currents that can be controlled [17]. The superior operating efficiency of a unit in the region where SiO_2 and HfO_2 overlap according to these explanations, in order to achieve a ratio of 5.5 x 10^{11} I_{ON}/I_{OFF} and a source overlap of 49.5 mV/dec, using SiO2 is remarkable as compared to using HfO2 when the gate dielectric is HfO_2[18]

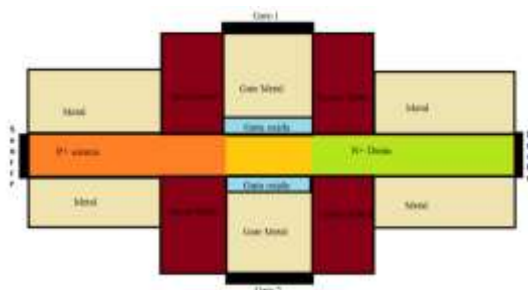

Fig.5. Double gate Tunnel FET

Arun Samuel et al.[19], which was used to evaluate the band-to-band manufacturing speed. The Double Steel Dual Gate TFET improves performance in many ways, including by increasing I_{ON} and decreasing leakage current. When compared with conventional devices, Anjani Devi N et al.[20] revealed that double core hetero junction TFET (DG-HTFET) enhances the SS by 2.45 times, I_{ON} is ~ 10^{-6} A/m, and I_{OFF} is 0.1 PA/m. Sanjay Kumar et al.[21] proposed the use of DM DG TFET in conjunction with HfO_2/SiO_2material. This invention was made possible by transporting the source to the channel as well as the drain to channel exhaustion zones. To accomplish superior results with regard to the I_{ON}/I_{OFF} ratio, ambipolar and SS of this device, the work function 4.4ev actions of the tunnelling and auxiliary gates of this structure have been improved. W.Li et al. [22], define the SS of doping substantially less DG-TFET as being greatly boosted by skillfully developing rear gate technology and bias is shown in Fig.6. The simulation results show that the device's conduction state, as determined by Germanium, contributes to an increase in the performance of the dual gate device.

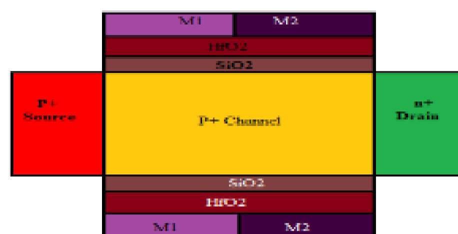

Fig.6. Double Metal Double Gate TFET model

M.venkatetesh et al.,[23] described Statistical modelling of a two-dimensional (2-D) vth is used to create dual halo gate stacked TMDG TFET with a fixed charge density at the HfO_2/SiO_2 stacked oxide interface. ON current (10^6A/m), I_{OFF} (10^{16}A/m), SS value 50mv/dec and In addition to this, the ratio of I_{ON} to I_{OFF} is 10^{10}. When the voltage applied to the input gate is raised, it can be seen quite clearly that the total electric field likewise rises at the same time. So, there is a direct link between the voltage applied to the gate input and the total electric field SnehSaurabh [24] In 2009, we saw the introduction of the lateral strained double gate TFET (SDGTFET). The whole silicon body of this device is strained silicon, which may be produced using single-layer strained SOI technology. This structure is comparable to the ordinary DGTFET.The completely overlapped device in [25] K.Kao et al. produces the maximum ON-currents; Differentiating between the three forms of TFET line tunnelling based on the ON-current. To a large extent,

it is dependent on two stylistic aspects in order to shorten the tunnel course. One of these is supply concentration, which causes smaller tunnel methods to shrink as a result of an improved electrical field.

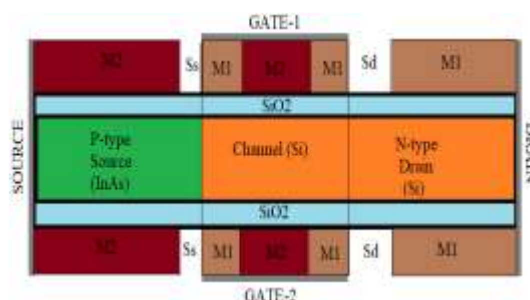

Fig 7. Hetero junction Double gate Dual metal Charge plasma TFET

Charge plasma diode is the dopingless device which is made with the charge plasma concept[26] is shown in Fig 7. To make p and n type region, two gates are implemented above intrinsic silicon. A dielectric layer also induced within gates and silicon. InAs material is employed to build a hetero charged plasma TFET (H-CPTFET) in order to shorten the lateral tunnelling distance at the source/channel contact[27]. The device provides a greater ON-current due to the increased BTBT generation rate made possible by the smaller tunnelling width at the source/channel junction. The first a DMCG-HCPTFET is introduced to better enhance ON-current.

Fin gate Tunnel FET (Fin TFET)

Ajaykumar D et al.[27-29]explain the engineered structure relies on substance variant with the usage of silicon substance for 3D Fin TFET structure by changing the fin-height is shown in Fig 8. The features are analysed together with the version in bone elevation and substance variation at various areas of this arrangement [30]. The drive current (I_D) of 18×10^{-6}A using a minimal leakage current of 10^{-15}A and SS of 25mV/decade.

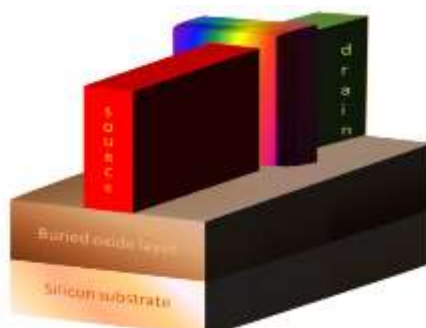

Fig 8. Rectangular Fin gate Tunnel FET

Kaishen Ou et al.[31] revealed the structure of a wrapped around epitaxial layer in a p-type Ge-Fin TFET. Gate source overlap length, drain doping, and equivalent oxide (HfO2)thickness are design consideration factors (EOT). Due to higher series resistance in the larger undoped epitaxial layer behind the gate, excessive gate-source overlap may restrict drive current. Ge growth at low temperatures (330–400 C) is favored. Woo Lee et al. [32] proposed GHG TFETs to advance the TFET switching activity. Thin bandgap materials are employed to improve the functioning of GHG TFETs. Both silicon and SiGe this TFETs have conduction currents of 3.8×10^{-8} A/m and 8.77×10^{-8} A/m, respectively. Triple-gate TFETs Encapsulated with an Epitaxial Layer The effect that a Si fin's height (H_{fin}) and width (W_{fin}) have on the transport properties of the epitaxial layer TFETs The vertical BTBT cross-sectional area is proportional to Hfin because the EL is created on the top and sidewall of a fin. As a result, a rise in H_{fin} results in an increase in the amount of ion boost in the case of EL TFETs. In their study, Jang Hyun Kim and colleagues [33] proposed that TFETs have a SiGe channel, a fin arrangement, and a raised drain to improve the efficiency of their electrical functioning. It has been shown that the ON-state present (I_{ON}) is increased by a factor of 24 times higher than that of the Si control set and also by a factor of 6 times higher than the SiGe management team. In comparison to the SiGe control group, the ambipolar current, denoted by IAMB, may be reduced by a factor of up to 900. Pankaj Kumar et al.,[34],Ge Source hetero setup is applicable for the n-type GoS-HTTFinFET. It has been noted that there is a considerable increase in tunnelling rate as a result of a bigger overlapped zone with the whole of the channel, and as a consequence, a higher tunnelling rate is achieved.

2. METHODOLOGY

To design the proposed architecture of dual metal gate hybrid device is illustrated in Fig.9.Improving the tunnelling mechanism for this purpose gate controlling over the channel has been increase to create the maximum ON-current (I_{ON}).The simulation results are required to verify the existing methods and also change the gate architectures to observe the performance of dual metal gate hybrid device

PROPOSED MODEL

The metal gates with varying work functions, with the gate closest to the source metal (M1) having a lower work function and the gate most comparable to the drain metal (M2) having a substantially greater work function. As a result, the gate transport efficiency dramatically improved by increasing the electron velocity and the lateral electric field along the channel at the interface of the two gate materials. The proposed twin metal fin gate doubles the device's efficiency when applied to a tunnel field effect transistor (FET). Progressive enhancement of potential, the tunnelling mechanism of drive current at the source and channel junction using a reduced gate metal work function on the source side junction is one way the double metal fin gate affects the device's performance. Hence, the metal gate M1 is the Control Gate, while the M2 is the Screen Gate.

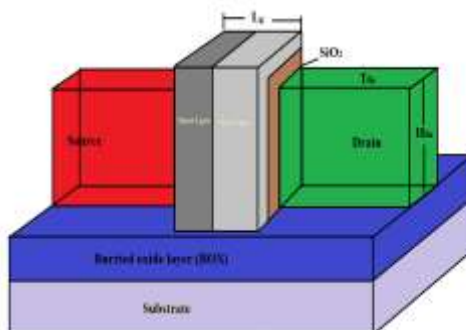

Fig.9 Double metal Fin TFET device structure

The source side of a dual metal gate TFET device is connected to the low work function (Φ_{M1}) gate material, while the drain side connects to the high work function (Φ_{M2}) gate material. A dual-material gate (DMG) is required, with materials M1 (near the source) and M2 (near the drain) having different work functions, Φ_{M1} and Φ_{M2}, respectively. A weaker drain-side electric field positively affects gate control in a DMG system. The potential under M1 is independent of the drain potential, as shown by the step potential. Simultaneously, the drain potential is not a limiting factor on the potential under M2.

3. SIMULATION RESULTS AND DISCUSSION

Design specifications of DM FinTFET source is doped with P-type concentration is 10^{20} cm^{-3} , lightly and moderately doped with n-type with concentration 10^{18} cm^{-3} and 10^{17} cm^{-3} . two metal gates are used in the device and its work functions are 4.7ev and 4.1ev . 40nm channel length ,40nm Fin thick ness and 20nm Fin height.Fig.10.shows mesh generated in DM FinTFET in TCAD simulation tool.

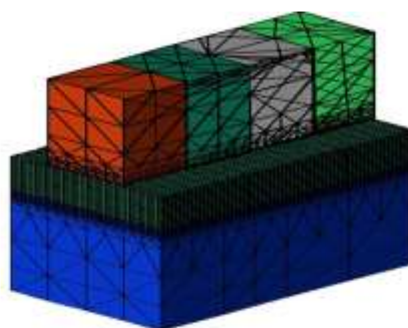

Fig 10. Simulated 3D architecture of Double metal FinTFET

A. Surface Potential characteristics of DM FinTFET

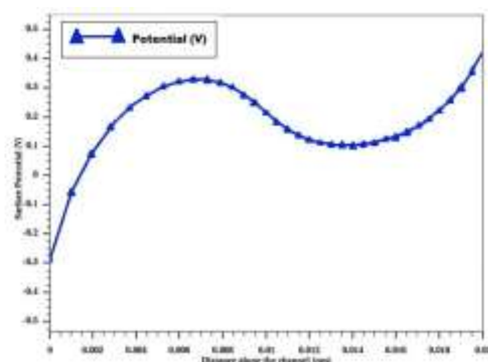

Fig 11. DM FinTFET Surface potential distribution along with channel distance at different V_{gs} and V_{ds}=0.1V

DM FinTFETs parallel to the channel length with a drain-to-source bias (Vds) of 0.1V. As the channel may be more precisely controlled by adjusting its gate, a higher gate-to-source voltage (V_{gs}) results in a higher potential across the channel is shown Fig 11. By selecting a suitable gate material on the source side, the screening effect of the DM FinTFET device may be amplified by increasing the source channel junction potential and promoting carrier tunnelling.

B. Electrical Characteristics of DM Fin TFET

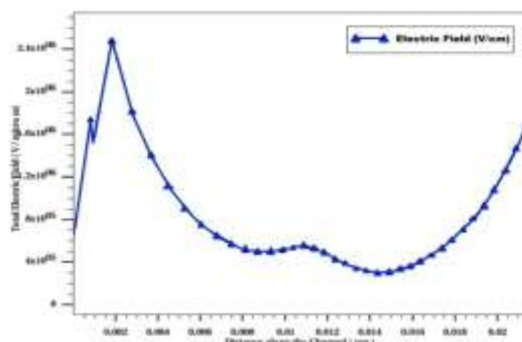

Fig 12. DM FinTFET Electric field characteristics along with distance of channel at V_{gs}=V_{ds}=0.1V

Fig.12 findings. The total electric field distribution at the source area of DM FinTFETs increases, indicating increased ON current characteristics, and falls at the channel-to-drain junction, indicating lower ambipolar current; both improve output current performance. For V_{gs}=V_{ds}=0.1V, the drain side work function is less than that of the source side gate. The overall electric field of DM FinTFET increases due to an increase in the tunnelling probability of the source side junction.

c. Input characteristics of DM FinTFET

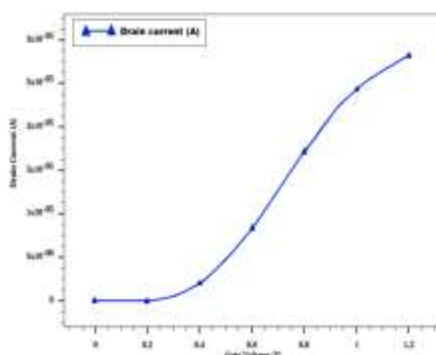

Fig 13. I_d – V_{GS} characteristics of DM Fin TFET

The fluctuation of the current-voltage characteristics of DM FinTFET devices shows in Fig. 13 for a Vds value of 0.1 V. Increased gate bias leads to improved tunnelling in the source-to-channel area, turn, causes an increase in

drain current. Kane's model uses to look at the peculiarities of the drain current. Eq.(1) for the BTB generation rate [21].

$$G_{BTBT} = DAE^{\gamma} \exp(-B/E) \quad (1)$$

C. Output characterizes of DM FinTFET

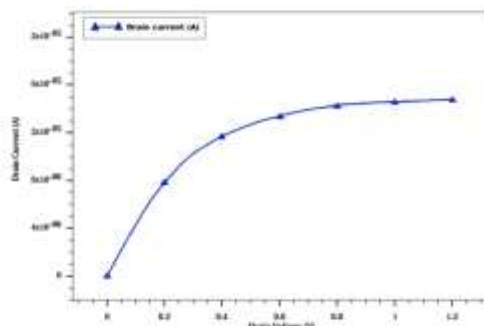

Fig 14. Output characteristics of DM Fin TFET structures. at V_{gs}=0.7V

Fig.14. depicts the I_d-V_{ds} curve for the DM FinTFET for a gate source voltage of 0.7 V. Double material gate FinTFET is possesses a high output current characteristics.

Table 1. Comparison of different gate structural TFET

TFET Structural		Device Parameters			
Model	Ref.no	SS $\left(\frac{mV}{dec}\right)$	$I_{ON}\left(\frac{\mu A}{\mu m}\right)$	$I_{OFF}\left(\frac{\mu A}{\mu m}\right)$	$\frac{I_{ON}}{I_{OFF}}$
SOI Fin FET	Ref.[1]	69	86	10-9	--
HJ tunnel TG FinFET	Ref.[14]	39	120	--	10^{10}
Gate field plate TFET	Ref.[12]	21.4	69	10^{-11}	10^{13}
2-source SOI TFET	Ref.[15]	120.8	10-^{11}	10^{-11}	1.1
PNPN L-gate N+pocketTFET	Ref.[16]	57.2	192.7	10^{-7}	10^{9}
SG TFET	Ref.[8]	57.3	52.6	25.2	10^{11}
	Ref.[10]	34.1	-	-	10^{7}
	Ref.[11]	47.2	-	-	10^{9}
DG TFET	Ref.[8]	41.5	10^{-9}	10^{-19}	10^{10}
	Ref.[17]	49.5	10^{-5}	10^{-16}	10^{11}
	Ref.[23]	35	10^{-4}	10^{-16}	10^{12}
Fin TFET	Ref.[5]	23.5	10^{-5}	10-^{12}	10^{9}
DM FinTFET	Proposed model	18.2	10^{-6}	10-^{15}	10^{9}

4. CONCLUSION

The article focused on the DM FinTFET hybrid structural model. DM Fin-gate TFET were suggested use of Sentaurus TCAD modeling will improve the performance of similar devices. Using this model, we can achieve low SS (18 mV/decade across four orders of drive current), high drive current (10^{-6} A/m at V_{DS} = V_{GS} = -0.5 V), and reduced low ambipolar flow of up to 10^{-15} A/m. Data from Sentaurus TCAD simulations are in excellent accord with the model's findings. Finally, it is stated that the DM FinTFET device, because of its increased performance, plays a critical role in high speed and low power applications for obtaining precise and dependable results.

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