Fiber Optical Communication Encoders :A Literature Review

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Abstract

As internet is unavoidable in our day to day life, there is a huge demand for high speed digital communications. Nowadays fiber optical communication is popularly used because it has good speed and bandwidth than other communication systems. Also Optical fibers offer high immunity to electromagnetic interference unlike copper wires as it is non-metallic. In this paper, many VLSI architectures of various encoders of optical communication are reviewed.

Keywords— Optical communication, encoder, VLSIarchitecture, FEC codes

1. INTRODUCTION

Invention of optical communication have resulted in improvement in data communication drastically all over the world. As the data is transmitted in the form of light, the speed of transmission is too high.

Fig 1., displays a simple architecture of optical system. The original input message to be transmitted is fed to FEC encoder. The encoder generates codeword by merging paritybits to input data. Then the light source emitter processes thecodeword and transmits in the fiber channel in the form of light. Then it enters into light receiver which converts the received light back to codeword. FEC decoder performsdecoding as well as error detection and correction to retrieveoriginal message.

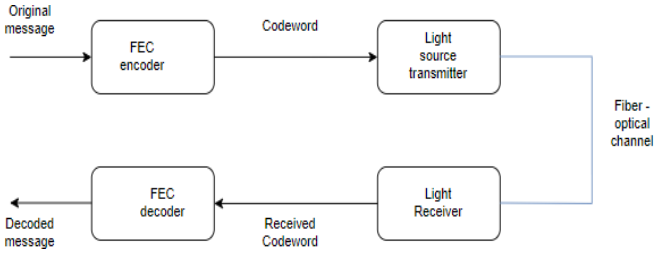

Fig. 1. Optical fiber communication system

Here, FEC encoder plays a major role in speed, area and totalpower consumption in overall optical system. In this paper, innovative architectures of various optical encoders proposedby different researchers are reviewed.

I. LITERATURE REVIEW

A. Staircase encoder for low power & area

An FEC encoder was proposed in the paper titled, "Area- and Power-efficient staircase encoder implementation for high-throughput fiber-optical communications". Staircase codes is one of the high performance FEC codes. It's 2D array representation is given in Fig 2.,

Initially zeroes are filled in block 0. Others blocks have information and parity bits. Grey colour represents information bits. White colour represents parity bits. The arrangement of data and parity bits look like staircase here. The data in staircase blocks moves into staircase encoder to get generated into codewords.

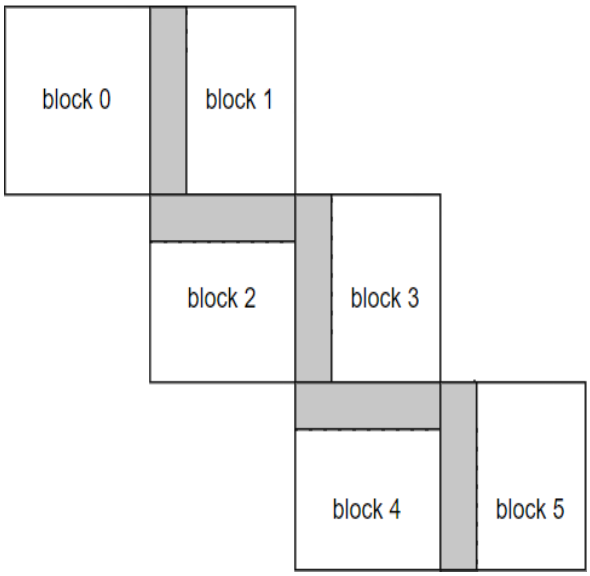

Fig. 2. 2D array representation of staircase codes

The architecture of staircase encoder is displayed in Fig 3., Here precomputed parity generation matrix is used. This matrix is splitted into P_a and P_b. They are stored in ROM.Input data (A) of current block and P_b^T are given to Bit-MatrixMultiplier. Bit-Matrix multiplier calculates partial parity bits(Ci). Then Bit-Matrix

Adder adds these partial parity bits (Ci) with the precomputed parity bits (C) to produce complete parity bits Ck. After that, the data formatter links the input data (A) with Ck to produce codeword (V).

Next the parity generation units takes this codeword (V) and Pa as inputs and forms partial barity bits (C+1). At the end complete parity bits (C) is generated, which will be used to encode next staircase block as shown in below figure.

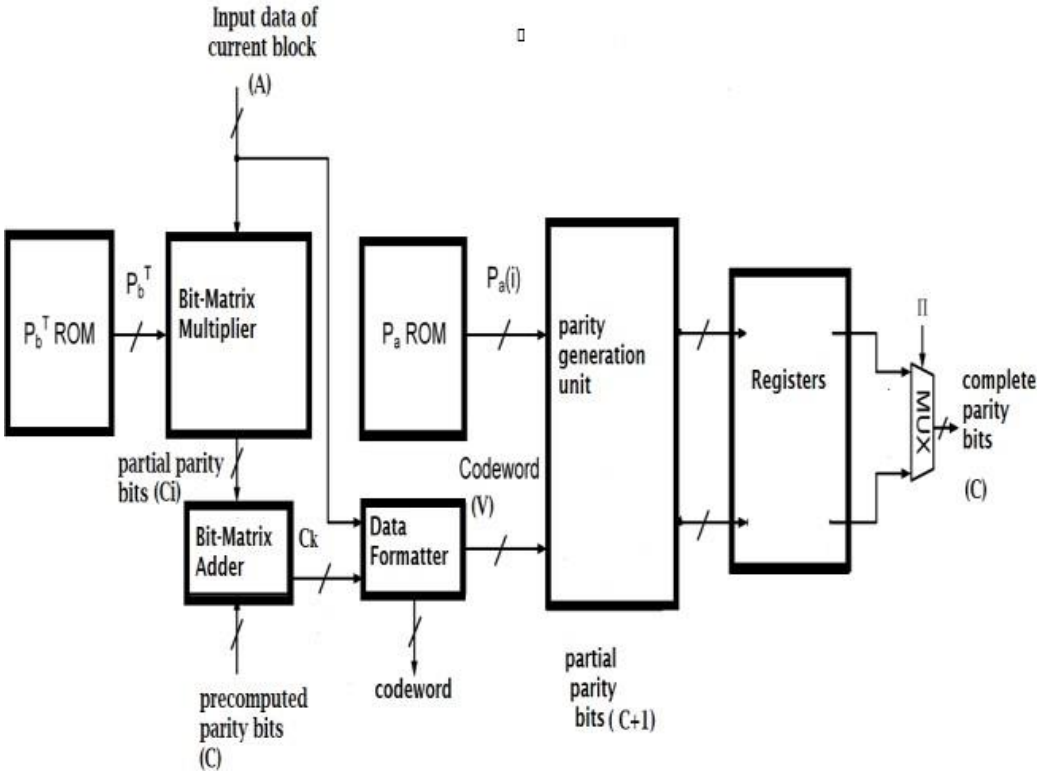

Fig. 3. Architecture of staircase encoder

This encoder takes only one clock cycle to process one row of staircase blocks. Hence the main advantage of this encoder is it takes very less time. The authors have designed this using 65 nm technology. As per results, the encoder can run at 909 MHz and it can attain the throughput of 432 Gbps as well as it can consume power upto 323-mW. Four clock cycles is the latency of this FEC encoder.

B. High speed Staircase Encoder

Guanghui Hu et. al., proposed a staircase encoder in the paper, "Beyond 100Gbps encoder design for staircase codes". The architecture is given below in Fig 4.,

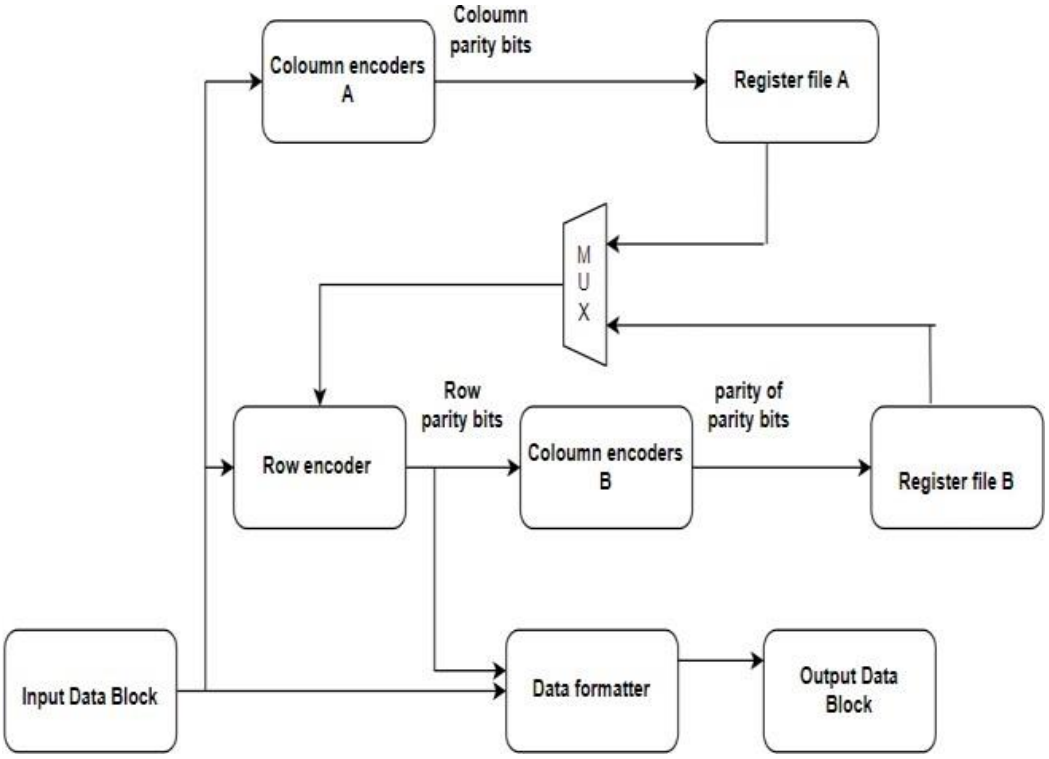

Fig. 4. Architecture design

The working is described as follows. Staircase code array is given in Fig 1., For example, when information bits of block1 (current input) is given as input, it passes through row encoder to get its parity bits and moves to output by data formatter as a codeword and simultaneously this information bits of block 1 also passes through column encoder to generate parity bits for block 2 (future input) in advance as shown in fig 4., Register file A saves the coloumn parity bits. Register file B saves the parity of row parity bits. The MUX gives the required input to row encoder.

After block 1, when a certain row of block 2 bits comes as input, the same process get repeated. Updating of block 2 parity bits continues, simultaneously encoding of block 2 also goes on. Thus this process continues for all blocks.

This staircase encoder shows high level parallel operation. Hence it has good speed. This is done using 90 nm CMOS technology. It can attain throughput of 119.5 Gb/s @ 500 MHz.

C. LDPC encoder

The authors have designed LDPC hardware encoder in the paper, "A flexible hardware encoder for systematic low-density parity-check codes" for LDPC codes using FPGA technology. It is shown in below figure.

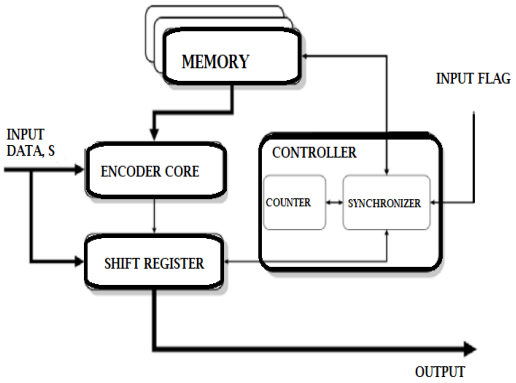

Fig.5. Architecture of LDPC encoder

In above architecture, the memory has block size, code rate information as well as the contents of parity sub- matrix (P^T). The block size represents the total number of bitsin the codeword. The code rate means the number of parity bits available and the number of parity bits have to be calculated to form a codeword. This code rate as well as block size goes as input to the controller. When an message is givenas input, controllers fetch the contents available in the memory and it transmits it to parity calculators. To calculate parity bit,binary vector multiplication of the message and one row of the parity submatrix, P^T need to be done. After parity calculation,the results are also saved in memory. After all parity bits arecalculated, the final codeword is generated by combining theinput message and calculated parity bits.

It attains throughput between 115Mbps and 360Mbps based on the block length.

D. BCH Encoder

The authors have designed an encoder for super FEC Codes in the paper, "10Gb/s Orthogonally Concatenated BCH Encoder for Fiber Communications". The encoding anddecoding of BCH codes is displayed figure below. The data are in G.975 framing format. They are mapped into theinternal frame. Then the data gets encoded by the column androw encoding modules. When encoding is finished, the data are remapped into G.975 frame format. After that, the data istransmitted through channel to the receiver side.

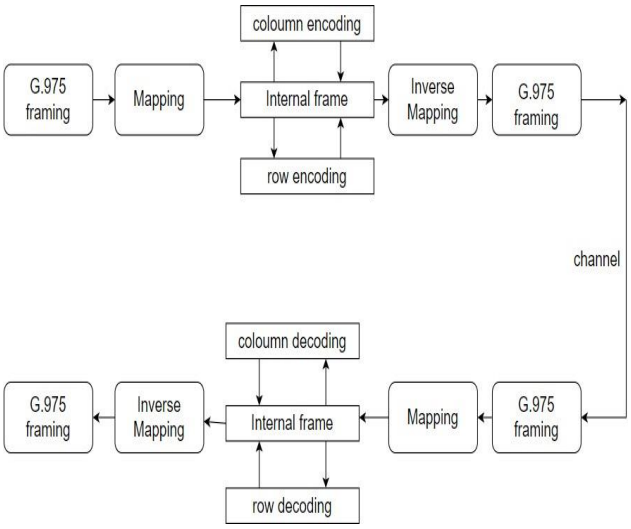

Fig. 6. Encoding & Decoding process

Internal frame structure is displayed in Fig 7., below., It has 900 32-bit columns. From 860th upto 899th coloumns arefor row parity. Row and column parity are zero, beforecodeword is generated.

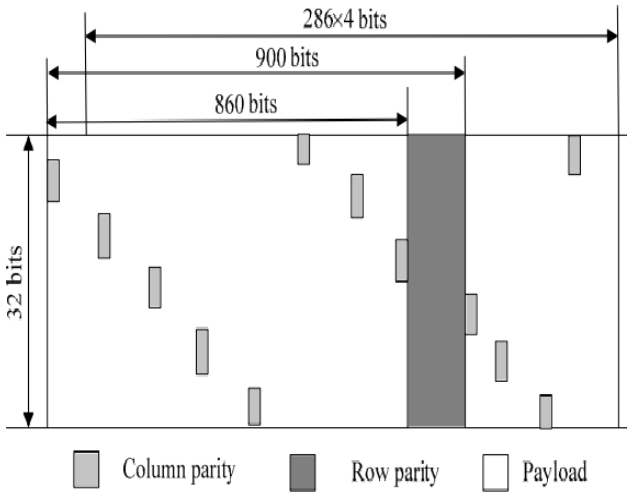

Fig. 7. Internal Frame Structure

Block diagram of encloding module is represented in Fig.8., below. Coloumn encoding module has 32 encoding groups. Each group consists of four 4-bit parallel encoders. In row encoding module, two encoding groups are there. Each group has sixteen 4-bit parallel encoders. For bufferingthe input data and for storing the parity bits, two types of RAMs are used.

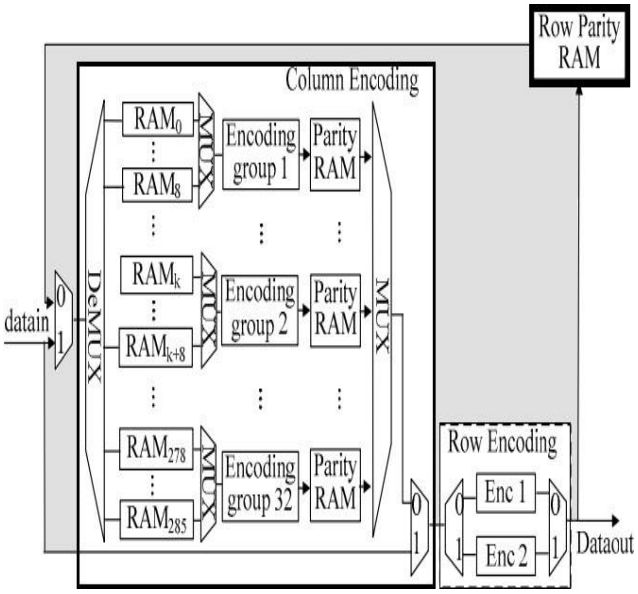

Fig. 8. Block diagram of encoding module

Data to be encoded and row parity bits are stored into RAMs first via Mux and Demux in the coloumn encoding module. MUX transfers only required data into encoding groups. After processing, the column parities are generated and stored in the parity RAMs which will be used for row encoding.

At Row encoding module, Enc 1 as well as Enc 2 function in a PingPang mode, i.e., , when Enc1 encodes, Enc2reads data, and vice verse. Thus row parity bits generated andgets stored in Row parity RAM.

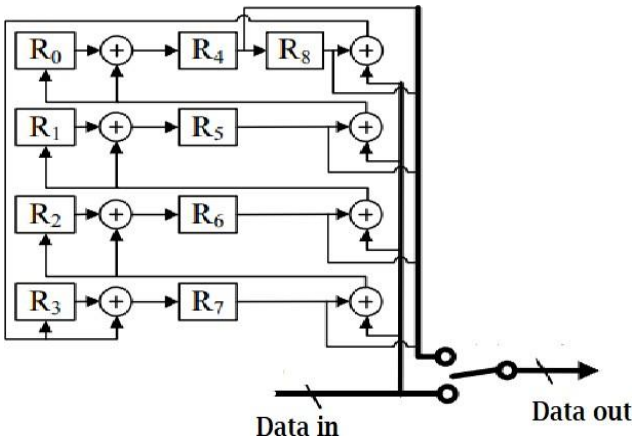

Fig. 9. Parallel BCH encoder

Both row and column encoding modules use 4-bitparallel encoder which is shown in above Fig 9., where R0,R1, R2 etc., represents registers. As serial LFSR encoder shown in Fig 10., takes large number

of cycles to encode, parallel BCH encoder is used. The results show that 10Gb/s data rate can be obtained at 156Hz frequency.

E. Scheme to minimize fanout in BCH encoders

A scheme to remove fanout bottleneck was designed in the paper, "Eliminating the fanout bottleneck in parallel long bch encoders". In traditional serial encoders shown in Fig 10., code word C(x) is produced by passing each bit of message input m(x) in the serial shift registers andmultiplying it by coefficients of generator polynomial g(x). Itrequires large number of cycles to generate codeword. It haslarge critical path and fanout bottleneck issue because outputof the right most exor gate moves as input to other exor gates.To overcome these difficulties authors have modified and developed parallel encoding scheme which block diagram isdisplayed in Fig 11.,

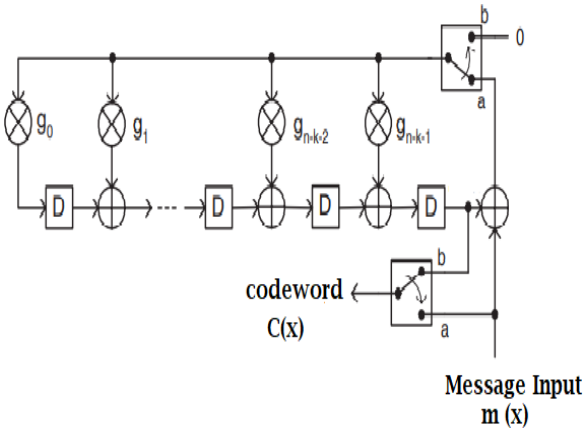

Fig. 10. Traditional serial LFSR encoder

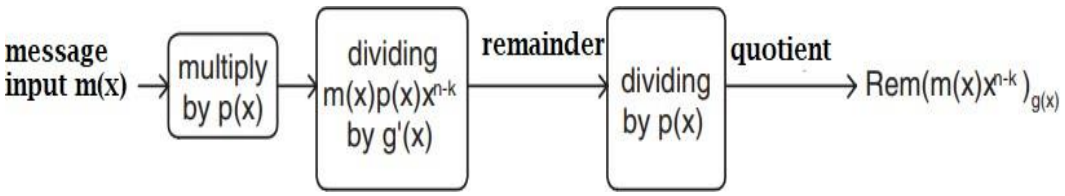

Fig. 11. Block diagram of modified encoding scheme

Step 1, step 2 and step 3 of this modified scheme is detaily given in the Fig 12., Fig 13., Fig 14 respectively. At step 1 input message polynomial m(x) is multiplied by a polynomial p(x). At step 2, remainder is calculated by dividing $m(x)p(x)x^{n-k}$ by modified generator polynomial g'(x). Both p(x) and

g'(x) can be calculated by Algorithm A which is written in pseudocode. At step 3, Quotient and reminder can be calculated by dividing the remainder from step 2 by p(x).

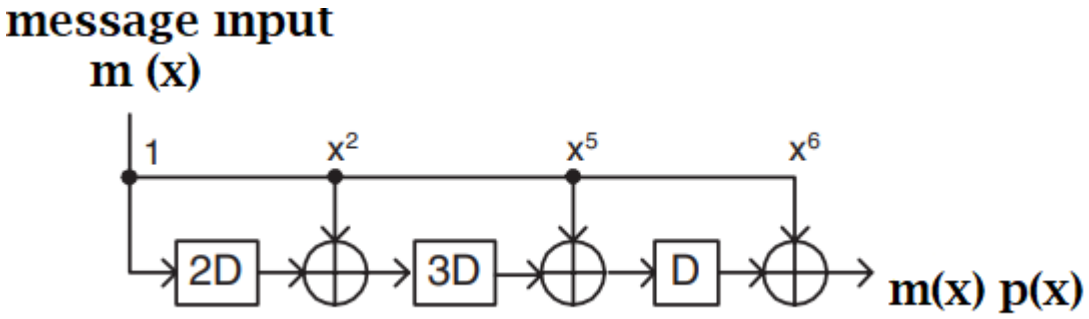

Fig. 12. Step 1 of modified encoding scheme

Rem(m(x)x^{n-k})g(x) represents the remainder polynomial. Atlast the remainder bits will be shifted out from the registersone by one to form systematic code word bits.

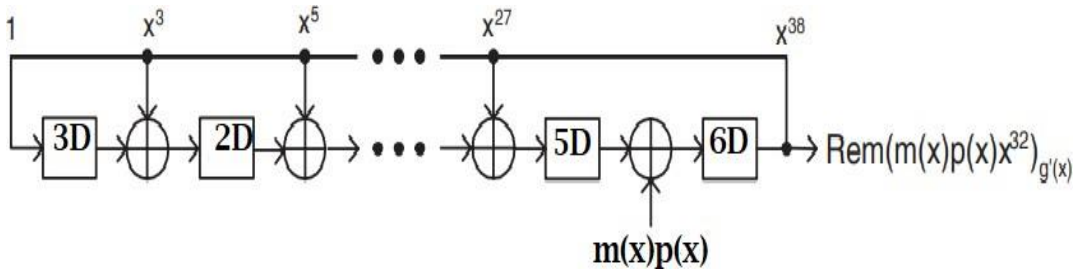

Fig. 13. Step 2 of modified encoding scheme

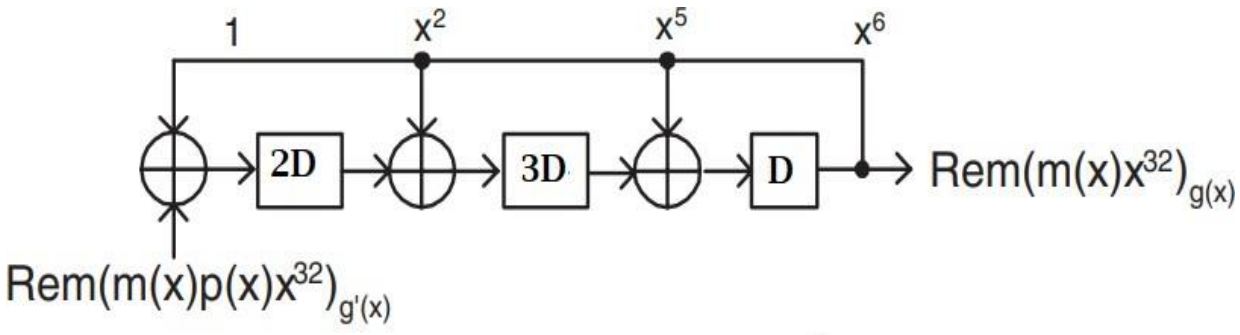

Fig. 14. Step 3 of modified encoding scheme

In this modified scheme, results showed that critical path is drastically reduced and the speed of operation is improved when compared to original parallel encoder. Hspice simulation is done with 0.35 µm library. Here 3.94ns is the estimated critical path.

F. QC-LDPC encoder

LDPC Codes are popular due to their good error correction capability. Usually traditional LDPC encoders use blockmemories, cyclic shifters, exor gates for encoding as shown in Fig. 15.,

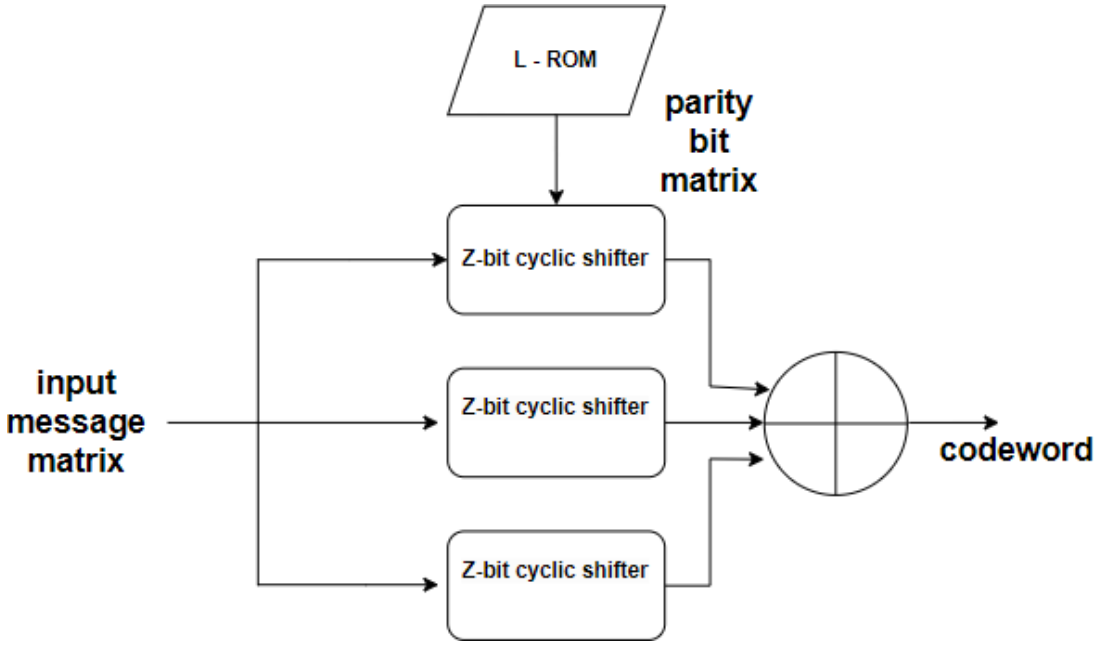

Fig. 15. Conventional method

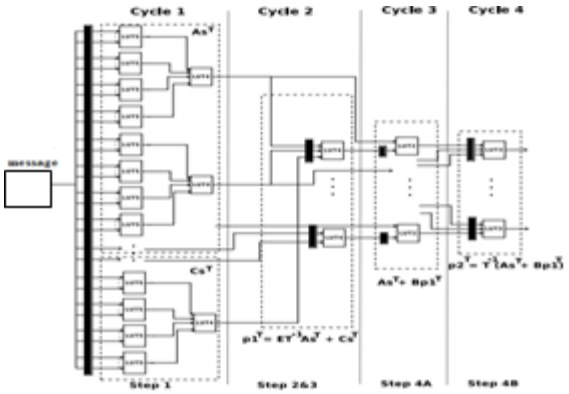

Fig. 16. Architecture overview

But in this paper, the authors have designed the encoder without these hardware components which is shownin Fig 16., Instead they have used LUTs. As no shift registersis present here, there will not be any shifting operations. Only hard-wire implementations is done.

So latency is increased as well as hardware resource utilization is very low. And an encoding algorithm proposedby S. Myung et al. in the paper “Quasi-Cyclic LDPC Codes for Fast Encoding” is

simplified and used. As per results, At290 MHz, it can attain throughput of 117.4 Gbps.

II. CONCLUSION

A comparative analysis of all reviewed encoders is givenbelow.

S.No	**Encoder Heading**	**Crresponding FEC code**	**Results**
1	Staircase encoder for low power & area	Staircase codes	432 Gbps @ 909 MHz
2	Highspeed staircase encoder	Staircase codes	119.5 Gbps @ 500 MHz
3	BCH encoder	BCH codes	115 Mbps and 360 Mbps based on block length
4	Scheme to minimize fanout in BCH encoders	BCH codes	10 Gbps @ 156 MHz
5	LDPC encoder	LDPC codes	3.94 ns critical path, throughput is 1
6	QC-LDPC encoder	LDPC codes	117.4 Gbps @ 290 MHz

TABLE I. COMPARISION

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