Application of Silicide Layer and Work Function in Optimization of MOSFET Process Parameters

Nitin Sachdeva[1], Neetu Gupta[2], Prashant Kumar[3], Rohan Bansal[4]

[1,2,3]Assistant Professor, Department of Electronics Engineering, [4]B.Tech Student

J.C. Bose University of Science and Technology, YMCA, Faridabad, India,

nitinsachdeva@jcboseust.ac.in

ABSTRACT

The optimization of a 45 nm NMOS device is investigated by applying silicide layer on Poly-Silicon Gate. This approach is utilized to investigate the device to analyze the electrical characteristics of the device. Silicides are generally chosen because of their appropriate electrical characteristics, such as low resistance, compatibility with silicon manufacturing processes, minimal to non-existent electro-migration, ease of dry etching, and good interaction with other materials. Silicide on the Poly-Si Gate electrode is used to reduce the Gate electrode resistance. The device is virtually fabricated with channel length of 45nm using ATHENA module of SILVACO and the electrical characteristics of the device are analyzed using ATLAS module of SILVACO. There are various materials that can be used as Poly-cide i.e silicide on Poly-silicon. In this paper, the comparative analysis of silicide process to increase the conductivity of Poly-Si gate. Four different materials are considered separately during the virtual fabrication of 45nm NMOS device. The platinum silicide has lowest OFF state leakage current equals to 6.06385nA after optimization approach.

Keywords: NMOS, EDA, TCAD, MOSFET

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1. INTRODUCTION

Over the last few years, semiconductor manufacturing has done notable progress and primarily leading to fast advancement in integration techniques as well as the design of large-scale devices. As the integration level of chip improves, there is more complication in manufacturing. The transistor size is switched from micrometer to nanometer. The development in solid-state electronics research in particular and semiconductor-based electronics trade began with the growth of bipolar transistors which is found to be one of the most significant innovations in 20th century. This innovation of bipolar devices had an extraordinary effect on the growth of the science and technology of semiconductors at that time. The bipolar junction transistors (BJTs) are replaced by MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) in Digital Electronic Circuits. This study aims to investigate the issues caused by

scaling the dimensions of MOSFET and applying alternative methods to manage them. Various architectures, channel materials and modified structures are suggested to solve the issues in existing devices. Different techniques are explored to reduce the leakage current.

There can be millions of transistors on a tiny piece of silicon in a modern-day IC. Of course, without computer aids, the manufacture and design of these ICs cannot be performed. Electronic Design Automation (EDA) tools involve both the manufacture and design of these ICs. Highly accurate software tools are needed to analyze and simulate embedded circuit design and manufacturing. Lots of research have been performed on these problems and are still going on. The whole work is done to accomplish this research work is performed in SILVACO TCAD Tool. ATHENA offers a platform for the simulation of ion implantation, diffusion, etching, deposition, lithography and oxidation of semiconductor materials. ATLAS simulates semiconductor electrical, optical and thermal behavior. ATLAS is a two and three-dimensional device simulator based on physics that analyzes the electrical behavior of semiconductor devices under defined bias conditions.

ATLAS uses the physical structures that are simulated with ATHENA as input. The combination of ATHENA and ATLAS enables the effect of process parameters on device features to be determined. Many simulations of the ATLAS tool are using two input files. The first input file is a text file containing ATLAS executable instructions. The second input file is a configuration file describing the simulated structure. ATLAS generates three kinds of output data. The first component of the output file is the runtime data which gives you feedback and alerts and error alerts as the simulation continues.

The output file's second form is the log file which contains all supply voltages and currents for system analysis. This tool initializes and manipulates the framework and offers fundamental installations for deposition and etching. ATHENA is usually used in combination with VWF INTERACTIVE TOOLS. DECK BUILD, TONYPLOT, DEVEDIT, MASKVIEWS and OPTIMIZER are the other tools. TONYPLOT provides capacities for scientific visualization. For MOS transistors, silicide gates have been suggested as a possible alternative to Polysilicon (Poly-Si) gates. They have greater conductivity and eliminate the gate-depletion effect, just like pure metals. Additionally, Poly-Si loses its advantage over metals in terms of thermal stability when high-K dielectrics are used to reduce gate leakage. Additionally, silicide replacement gates provide more advantages for process integration than metal gates [1].The elf-aligned silicide (SALICIDE) technology has been extensively used to lower polysilicon gates' resistance. Silicon is deposited initially to safeguard the underlying gate dielectric during future metal depositions and etches. Metal dry etch can be avoided because silicides can be formed via a salicide reaction between silicon and metal. As channel length is scaled, gate resistance

increases. So to reduce the gate resistance, silicidation process is used [2].

2. METHODOLOGY

A 45nm NMOS is designed and virtually fabricated in Athena using substrate doping concentration of 5e15 cm^{-3}. Then this device is simulated in ATLAS of SILVACO device simulator using different silicides i.e Titanium silicide, Cobalt Silicide, Platinum silicide and Tungsten Silicide. Various electrical parameters like Threshold voltage, ON current, OFF current, Substrate current, DIBL and Sheet resistance.

Table 1: Specifications of 45nm NMOS

Device Parameters	**Value Undertaken**
Effective Gate Length, L_G	40nm
Gate oxide thickness, t_{ox}	1nm
Substrate doping, N_A	5e15 cm^{-3}
Supply voltage, V_{DD}	1.2V
P well implant	1e12 cm^{-3}
Threshold adjust implant	5e12 cm^{-3}
S/D Doping	$3.5x10^{15}$ cm^{-3}
Halo doping	5e13 cm^{-3}

The device is virtually fabricated in SILVACO ATHENA using specifications mentioned in the Table 1. NMOS device with effective channel length of 40nm has been designed using user-defined specifications. Effective gate length is considered as 40nm with 1nm gate oxide thickness. The threshold implant and S/D doping considered $5x10^{12}$ cm^{-3} and $3.5x10^{15}$ cm^{-3} respectively with 1.2V supply. Also, lightly doped substrate is chosen and halo doping is done to reduce the short channel effects.

3. SIMULATION RESULTS

To ensure that the resistance offered is small, silicide is deposited on the top of the surface [3]. The titanium reacts with silicon (i.e. single crystal silicon in the source and drain region, and poly-crystal gate region) and forms titanium silicide. It does not react with silicon dioxide. The structure of 45nm NMOS with Titanium silicide as silicide on Poly-Si gate is shown in Figure 1 below:

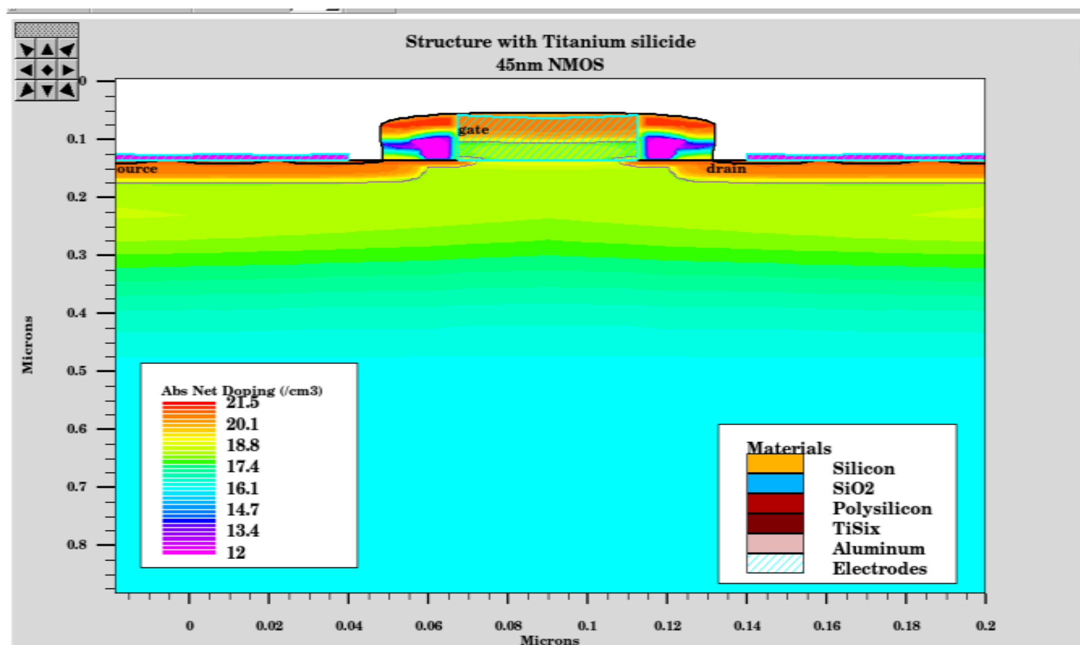


Figure 1 Structure of 45nm NMOS with Titanium Silicide

In the next step, the unreacted titanium is removed by wet chemical etching. This process is called silicidation [4]. Same process is followed for Cobalt, Platinum and tungsten. Work-Function Engineering is used to reduce OFF state leakage current in lightly doped substrate devices. The work function is a significant parameter in device. Lightly doped substrates provide greater leakage current but with the gate work-function variation of 4.0-4.4eV, less leakage current is achieved in OFF state. The work function of the gate material is considered 4.12eV. The poly-silicon gate was then laid and defined followed by the halo implantation. When the silicide layer is deposited on Poly-Si gate, the resistance of the gate decreases to 52.8154Ω/sq in platinum silicide as compared to without silicide Poly Si gate equals to 66.4958 Ω/sq.

Table 2 Performance Table when φ=4.12eV

Parameter	Titanium	Cobalt	Platinum	Tungsten
Ion (μA)	2850	2878	2849	2851
Ioff (nA)	6.06159	6.06812	6.06385	6.06255
Isub (A)	9.354 4e-07	9.68554e-07	9.30979e-07	9.35697e-07
DIBL (mV/V)	51.967	51.9574	51.9652	51.9661
Rs(Ω/sq)	60.4962	89.1988	52.8514	55.4345

The silicide layer is deposited at 910°C temperature at 0.005 seconds having the thickness of silicide of 25nm[5]. The extracted results after the simulation of device are shown in Table 2 above. The device is designed and simulated with different silicide materials and without silicide and the results is shown in following figures.

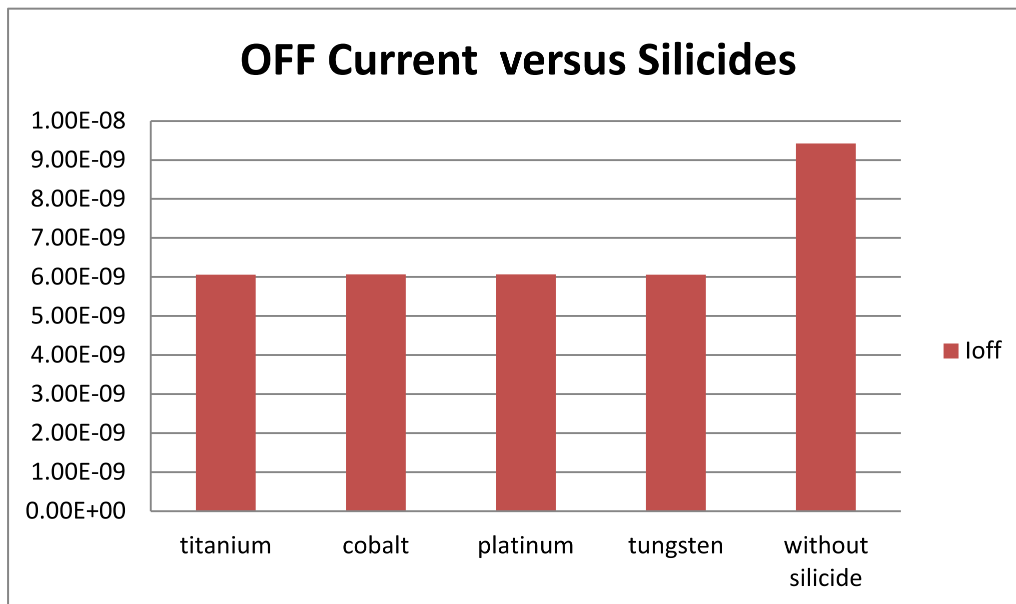
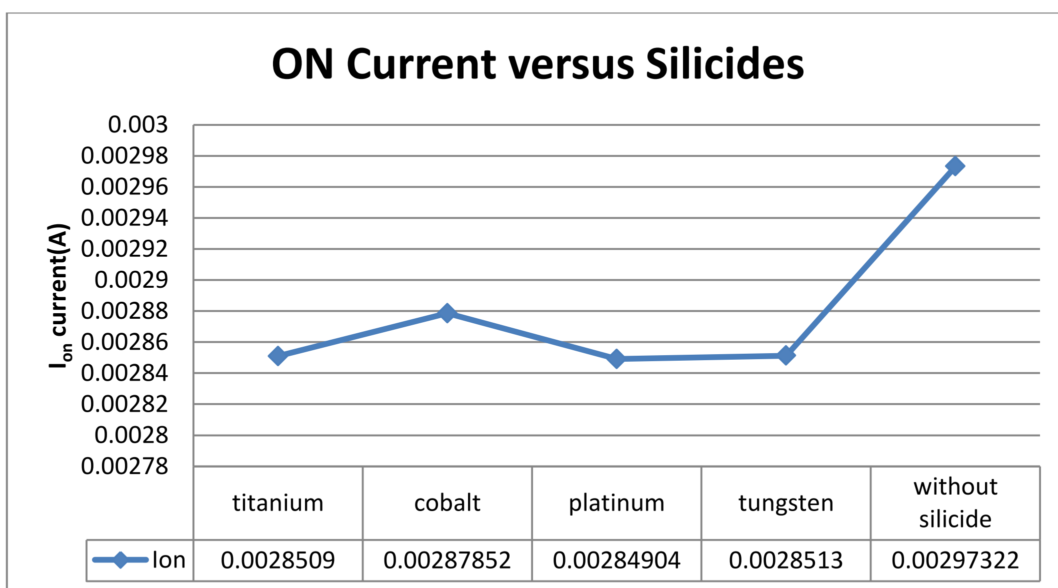


Figure 2 Variation of I_{off} current with different Silicides

The OFF state leakage current has been observed lowest of Titanium silicide equals to 6.06159nA and highest of cobalt silicide equals to 6.06812nA as shown in Figure 2 above. The OFF current without silicide layer is 9.422nA which is highest as compared to all silicide materials[6].



	titanium	cobalt	platinum	tungsten	without silicide
Ion	0.0028509	0.00287852	0.00284904	0.0028513	0.00297322

Figure 3 Variation of I_{on} current with different Silicides

The ON current has been observed lowest of Platinum silicide equals to 2849µA and highest of cobalt silicide equals to 2878µA as shown in Figure 3 above

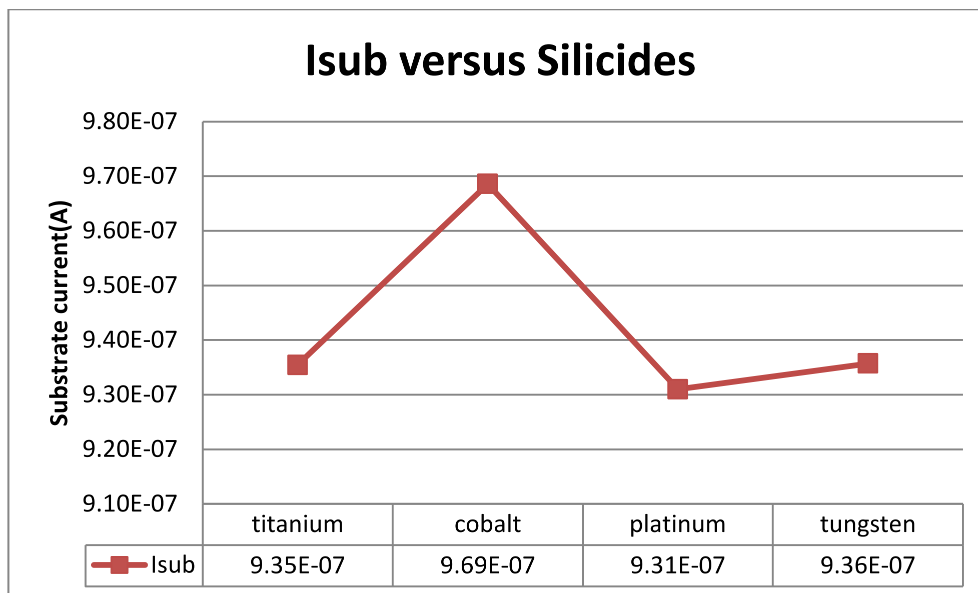


Figure 4 Variation of Isub current with different Silicides

From the simulation results shown in Figure 4, the cobalt silicide has very high substrate current as compared to other silicides and the gate with Platinum silicide has minimum substrate current equals to 9.31E-07A.

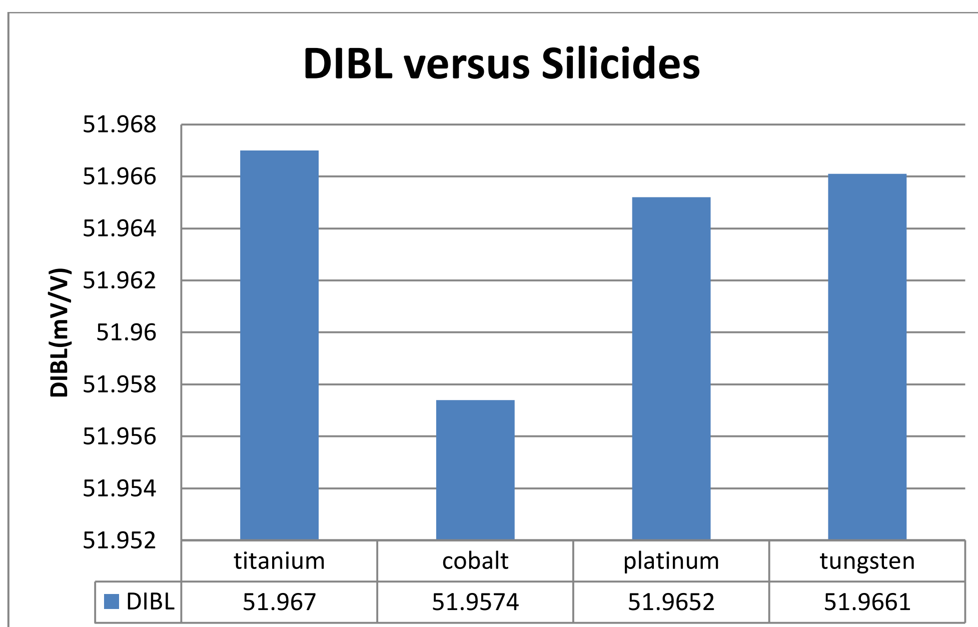


Figure 5 Variation of DIBL current with different Silicides

From Figure 5 above, Titanium silicide has highest DIBL leakage current.

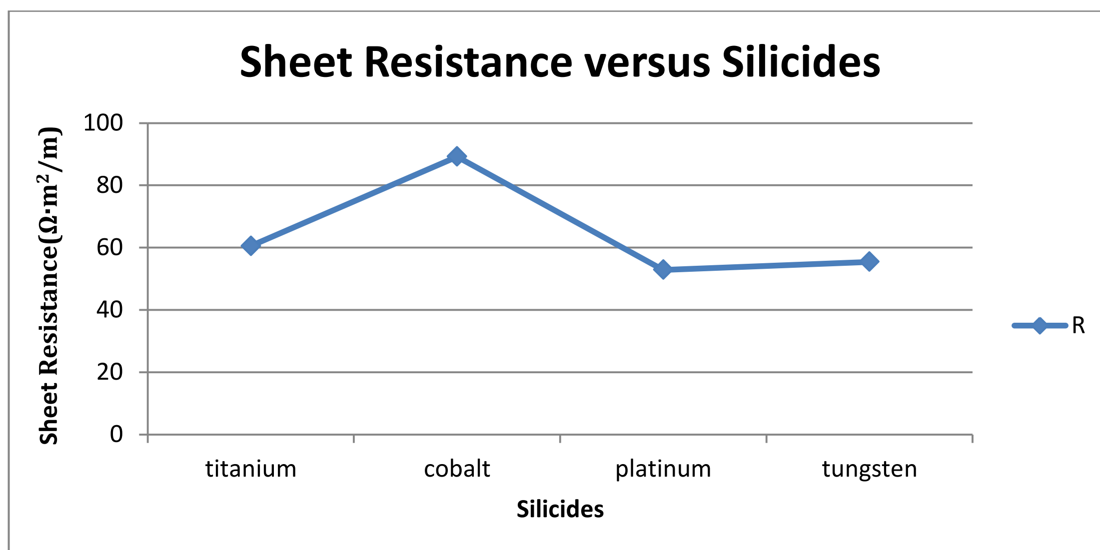


Figure 6 Variation of Resistance current with different Silicides

The nominal sheet resistance is in the order of 20 Ω/sq to 100 Ω/sq. To reduce the sheet resistance a silicide layer is deposited on the top of the polysilicon.The resistance of Poly-Si of cobalt silicide is highest among other silicides [7].

4. ANALYSIS WITH INCREASED WORK-FUNCTION OF GATE ELECTRODE

The work-function of the gate electrode is increased from 4.12eV to 4.16eV to analyze the effect of work-function on silicide coated gate [8]. The performance parameters are shown at 4.16ev work-function are shown in Table 3 below. It has been observed that if the work-function increases, OFF current, Substrate current and DIBL reduces. With these lowest leakage components, designed device can be used for low power applications.

Table 3 Performance Table when wf=4.16eV

Parameter	**Titanium**	**Cobalt**	**Platinum**	**Tungsten**
I_{on}	2692µA	2717µA	2690µA	2714µA
I_{off}	1.6596nA	1.66139nA	1.66022nA	1.73409nA
I_{sub}	8.76087e-07A	9.05216e-07A	8.7213e-07A	8.98155e-07A
DIBL	50.4235(mV/ V)	50.4139(mV/ V)	50.4217(mV/ V)	50.2539(mV/ V)

The various parameters of the device is calculated by the application of various silicide layers and their performance has been shown in the above Table 3

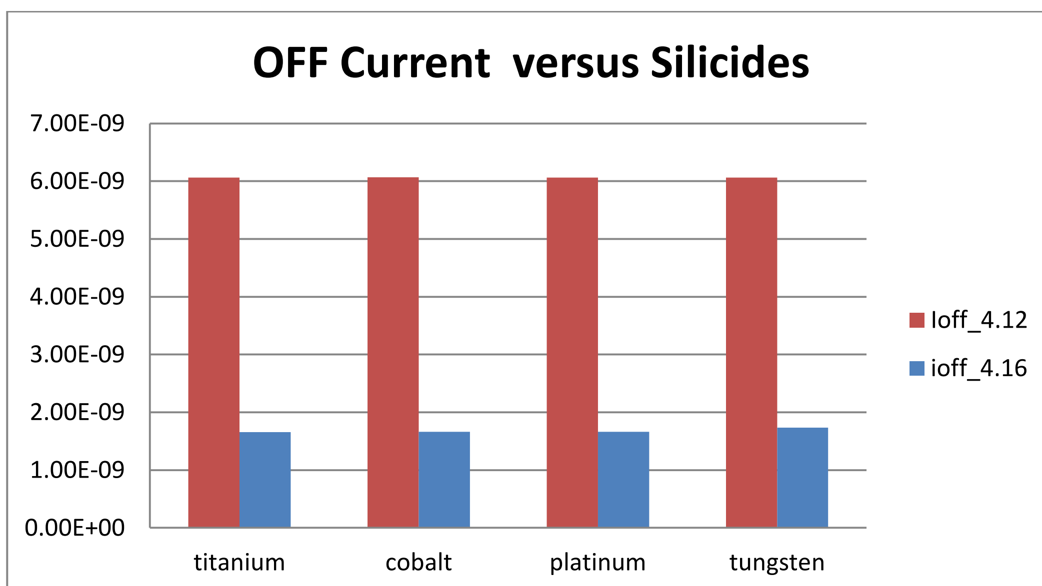
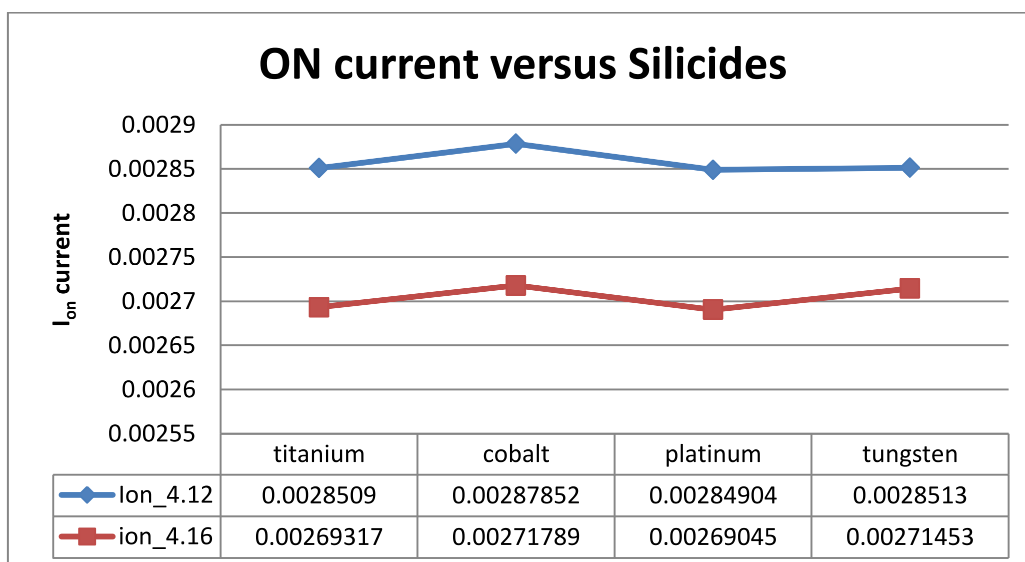


Figure 7 Variation of OFF current with different work-functions

As we increase the work-function of the gate, the OFF state leakage current decreases respectively of all the devices with different silicide materials as shown in Figure 7[9, 10].



	titanium	cobalt	platinum	tungsten
Ion_4.12	0.0028509	0.00287852	0.00284904	0.0028513
ion_4.16	0.00269317	0.00271789	0.00269045	0.00271453

Figure 8 Variation of Ion current with different work-functions

The device with platinum silicide has lowest OFF current for both work-functions as shown in Figure 6 above. The ON current variation with increased work-function is shown in Figure 8 above. It has been observed from the results shown in Figure 9 below that as the work-function is increased to 4.16eV, the

substrate current of the device decreases.

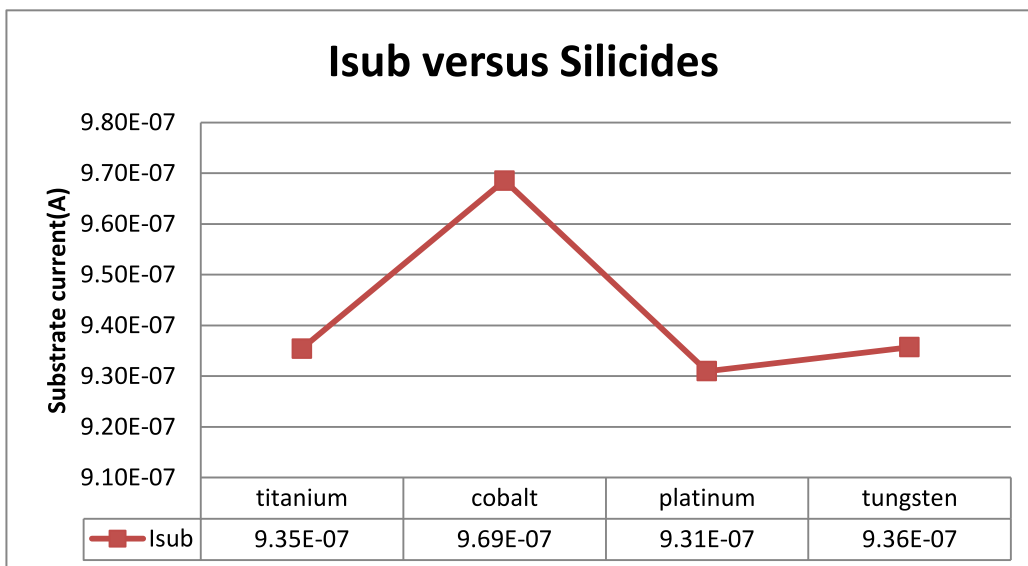


Figure 9 Variation of Isub current with different work-functions

As the threshold voltage of the device increases with the increase in work-function, DIBL decreases as shown in Figure 10 below.

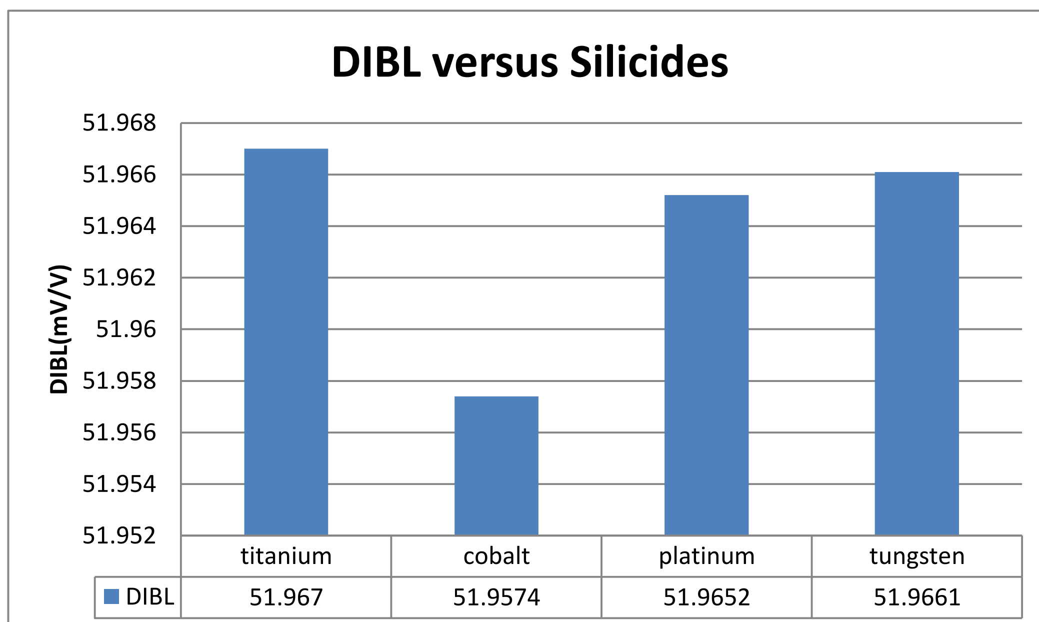


Figure 10 Variation of DIBL with different work functions

5. CONCLUSION

The transistor has been virtually fabricated using ATHENA module; simulated using ATLAS module of SILVACO and the electrical characteristics has been obtained. Poly-silicon sheet resistance should also be kept as low as possible to increase the speed of the device by shortening the time to accumulate

charge in the channel for a transistor to turn-on. This paper concludes the comparative analysis of various silicides on Poly-Si gate. It has been observed that Cobalt silicide has highest ON current equals to 2878μA but lowest DIBL equals to 51.9574mV/V among all. The platinum silicide has lowest OFF state leakage current equals to 6.06385nA and substrate current equals to 9.30979e-07A. The inclusion of silicides with Poly gate depends on the application of the device. All the results are also compared with gate without silicide layer.

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