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# DESIGN OF POWER EFFICIENT VEDIC MULTIPLIER BASED ON RL

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## Abstract

Reversible logic saves electricity. Reversible logic loses no information and creates unique outputs for defined inputs. No bits are lost, reducing power consumption. In this study, a novel architecture for a high-speed, low-power, and area-efficient 8-bit Vedic multiplier is described and implemented utilizing reversible logic to yield low-power products. UT Sutra produces partial product and sum in a single step with fewer adders than a traditional booth and array multipliers, reducing latency, space, and power consumption. A 4-bit Vedic multiplier plus modified ripple-carry adders create an 8-bit Vedic multiplier. The suggested logic blocks use Verilog HDL and Xilinx ISE for simulation.

**Keywords:** Reversible Logic gates, Ripple carry Adder, Urdhva Tiryagbhyam Sutra, Vedic Mathematics.

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## 1. Introduction

As technology advances, design requirements and complexity alter. Digital system design prioritizes power consumption. In irreversible logic, heat from computing is caused to the destruction of information (erasing bits of information), not the processing of bits. Landauer proved that every bit of information destroyed during an irreversible logic operation generates KTln2 joules of heat energy, where K is the Boltzmann constant and T is the system's temperature in Kelvin. The heat generated by the loss of one bit of information is small at room temperature, but when the number of bits is high, as in high-speed computational works like multiplication, convolution, Fourier calculations, and signal processing, the heat dissipated by them will be so large that it affects performance and reduces component lifetime.

Reversible computations lose no information and employ reversible gates. Using reversible logic decreases power consumption and improves system reaction time. Bennett established that reversible circuits prevent energy loss in a circuit. Reversible logic prevents information loss and power waste. Reversible computing doesn't need deleting information, thus it doesn't waste energy.

Thus, reversible logic circuits prevent energy loss by recycling the system's energy. Fan-out and gate output-to-input feedback are not allowed in reversible circuits. Due to these limits, reversible circuits may be synthesized backward. The input and output vectors are identical. In an n-output reversible gate, output vectors are 0 to 2n-1 permutations.

**Literature Survey**

For this investigation we have selected some papers as a reference study which are mentioned in further part of research paper.

Landauer, R. (1961) [1] argued that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function. This dissipation serves the purpose of standardizing signals and making them independent of their exact logical history. Two simple, but representative, models of bistable devices are subjected to a more detailed analysis of switching kinetics to yield the relationship between speed and energy dissipation, and to estimate the effects of errors induced by thermal fluctuations.

Bennett, C. H. (1973) [2] shown that such machines may be made logically reversible at every step, while retaining their simplicity and their ability to do general computations. This result is of great physical interest because it makes plausible the existence of thermodynamically reversible computers which could perform useful computations at useful speed while dissipating considerably less than kT of energy per logical step. In the first stage of its computation the logically reversible automaton parallels the corresponding irreversible automaton, except that it saves all intermediate results, thereby avoiding the irreversible operation of erasure. The second stage consists of printing out the desired output. The third stage then reversibly disposes of all the undesired intermediate results by retracing the steps of the first stage in backward order (a process which is only possible because the first stage has been carried out reversibly), thereby restoring the machine (except for the now-written output tape) to its original condition. The final machine configuration thus contains the desired output and a reconstructed copy of the input, but no other undesired data. The foregoing results are demonstrated explicitly using a type of three-tape Turing machine. The biosynthesis of messenger RNA is discussed as a physical example of reversible computation.

Kunchigi, V., Kulkarni, L., & Kulkarni, S. (2012, March) [7] proposed High speed pipelined multiplier architecture. The pipelined architecture consists of 3 stages. 1st stage consists of the 4 - bit Vedic Multiplication unit. 2nd stage consists of partial products and carry. 3rd stage consists of adders and the result of the multiplication. They presented the efficiency of Urdhva Tiryagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. The proposed algorithm is modeled using Verilog, a hardware description language. It is found that 11 logic cells are required to build nibble multiplier. The propagation time of the proposed architecture is found to be 4.585ns. Implementation has been done for the Xilinx FPGA device, Spartan-3E. The results show that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures.

Viswanath, L. Ponni. M, (2012) [8] considered reversibility plays an important role when energy efficient computations. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. They proposed a reversible design of a 16 bit ALU. This ALU consists of eight operations, three arithmetic and five logical operations. The arithmetic operations include addition, subtraction, multiplication and the logical operations include NAND, AND, OR, NOT and XOR. All the modules are being designed using the basic reversible gates. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits is also carried out.

Raju, B. R., & Satish, D. V. (2013) [9] presented A high speed complex 16 *16 multiplier design by using Urdhva Tiryagbhyam sutra. By using this sutra, the partial products and sums are generated in one step which reduces the design of architecture in processor's. By using this sutra, we can reduce the time with high extent when compare to array and booth multiplier. It can be implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT) filtering and in microprocessors. By using this method, they reduced the propagation delay in comparison with array based architecture and parallel adder based implementation which are most commonly used architectures. The main parameters of this paper is propagation delay and dynamic power consumption were calculated and found reduced. Saligram, R., & Rakshith, T. R. (2013, April) [10] proposed novel design of Multiplier. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryagbhyam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper we aim to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.

Thapliyal, H., & Srinivas, M. B. (2005, October) [11] proposed a "TSG" gate and is used to design efficient adder units. The proposed gate is used to design ripple carry adder, BCD adder and the carry look-ahead adder. The most significant aspect of the proposed gate is that it can work singly as a reversible full adder i.e. reversible full adder can now be implemented with a single gate only. It is demonstrated that the adder architectures using the proposed gate are much better and optimized, compared to their counterparts existing in literature, both in terms of number of reversible gates and the garbage outputs.

In present study, a novel architecture for a high-speed, low-power, and area-efficient 8-bit Vedic multiplier is described and implemented utilizing reversible logic to yield low-power products. UT Sutra produces partial product and sum in a single step with fewer adders than a traditional booth and array multipliers, reducing latency, space, and power consumption. A 4-bit Vedic multiplier plus modified ripple-carry adders create an 8-bit Vedic multiplier. The suggested logic blocks use Verilog HDL and Xilinx ISE for simulation

**Reversible Logic And Gates**

Reversible logic offers a way to build computers without heat dissipation. Reversible logic reduces teat creation owing to knowledge loss. Reversible logic makes computations time-invertible. An in reversible circuit has n inputs and n outputs, with each input pattern translating to a distinct output pattern. Garbage outputs (GO) of reversible logic are optimization and performance factors that do not contribute to the design. Quantum cast (QC) is the circuit's cost per primitive gate. The function's gate count (NG) is the number of reversible gates. Gate level is the number of layers needed to implement logic functions.

Features and design constrain of reversible logic.

- Equal inputs and outputs characterize reversible logic.
- No fan-out.
- No feedback loops.
- Unused outputs are trash signals.
- Reduce the number of constants at gate inputs.

Basic reversible gates used in the design are listed below:

**1. Feynman Gate (FG)**

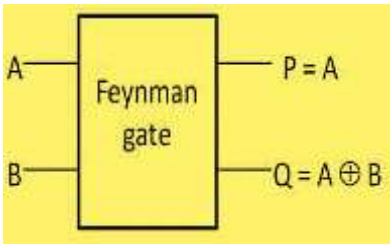


Figure 1: Feynman Gate (FG)

**2. Toffoil Gate (TG)**

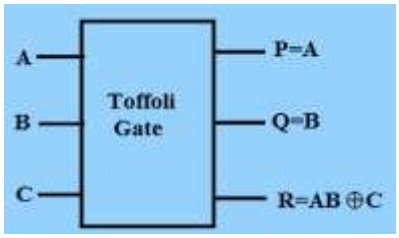


Figure 2: Toffoil Gate(TG)

**3. Peres Gate (PG)**

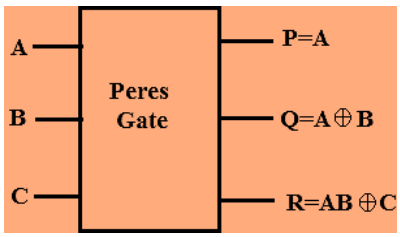


Figure 3: Press Gate (PG)

**4. HN Gate**

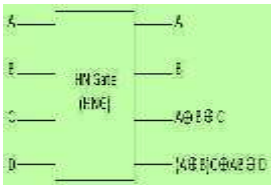


Figure 4: HN Gate (HNG)

## 4.0 Vedic Multiplier

Vedic math is faster than other multiplication designs. Vedic mathematics uses basic, fast arithmetic principles. It offers complicated calculation algorithms.

### 4.1 Urdhva Tiryagbhyam Sutra

The proposed 8-bit multiplier uses the UT sutra (algorithms). "Vertically and crosswise" is Urdhva Tiryagbhyam. "Sthapatya- Veda" (a supplement to "Atharva Veda") recognizes this UT sutra. This sutra multiplies two decimals. This sutra is applied to the binary number to make the algorithm digital. It's easier than traditional multiplication. Urdhva Tiryagbhyam Multiplication Algorithms are generic multiplication formulas. "Vertically and Crosswise" Multiply the two ends of the line and add the preceding carry. All results from many lines are added with the preceding carry. The least significant digit of the sum is one of the outcome digits, while the rest carry the next step. The carry bit is initially 0. It's quicker than array and
booths algorithms. "NxN" multiplier needs "NxN" AND gates, "Nx(N-2)" full adders, and "N" half adders. Vedic multiplier needs (N-1) adders. Figure 4 displays 4-Bit Vedic multiplier stages.

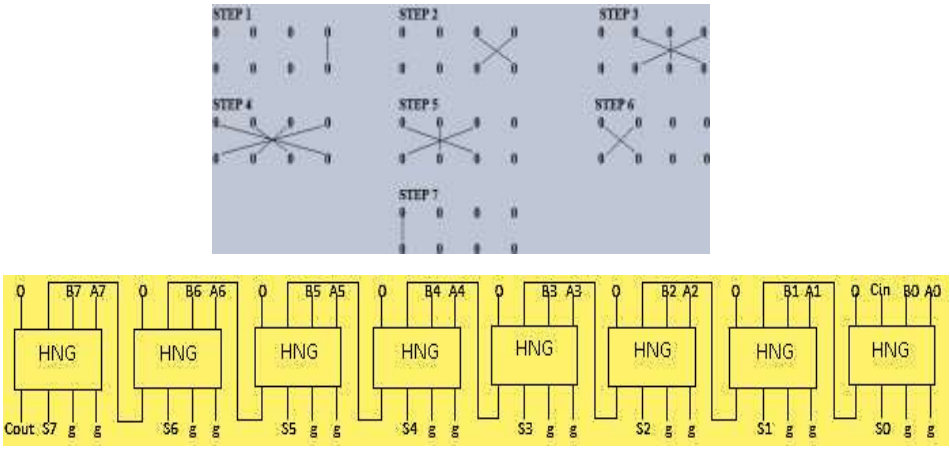


Figure 5: Vedic Multiplication Steps

## 5.0 Proposed Architecture

A reversible 8x8 Vedic multiplier has been developed, and it would provide a 16-bit binary output after multiplying two binary values. In the process of developing the multiplier, both Peres gates and Feynman gates are used. The development of incomplete products and additions being done simultaneously is one of the most attractive aspects of UT design.

Figure 6 depicts the proposed block diagram for the 8x8 Vedic multiplier. It is simple to implement because of the utilization of three 8-bit ripples carry adders and four 4x4 Vedic multipliers. In comparison to multipliers of the array and booth types, the architecture of this suggested 8x8 multiplier is quite straightforward and makes excellent use of resources. Reversible PG and TG gates are used in the construction of each and every multiplier. In addition, RCA is constructed using HNG gates. Therefore, the patterns

may be used in either direction. The quantum cost of this item is 720.

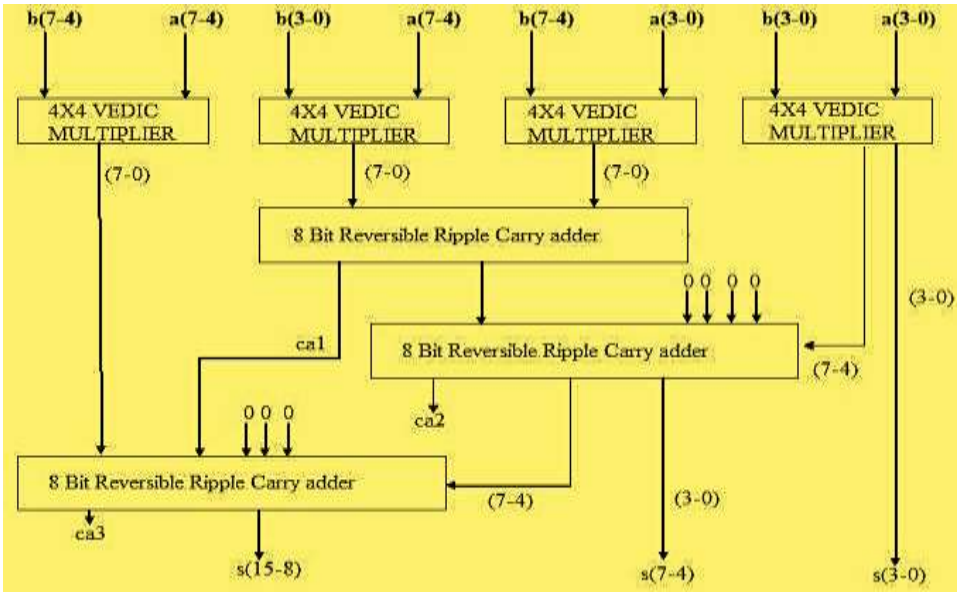


Figure 6: Proposed 8x8 Vedic Multiplier

An HNG gate will be used in the construction of a planned reversible adder. In the HNG gate, if the fourth input, D, is made to have a constant value of zero, and inputs are given through A and B and carried to the third input C, then it acts as a reversible one-bit full adder, and output is taken from R and S respectively. This occurs if the inputs are given through A and B and carried to the third input C.

An HNG gate with two 8-bit inputs and a carrier that is propagated from the list a significant bit (LSB) to the most significant bit (MSB), also known as a ripple carry adder, are used to produce the proposed 8-bit reversible adder. The MSB is the bit that is considered to be the most significant. The reversible ripple carry adder has a relatively tiny footprint, and its construction is quite straightforward; hence, ripple-carry adders are often used for cascade purposes. To construct an 8-bit ripple carry adder, you will need a total of eight HNG gates since each HNG gate performs the function of a complete adder for only one bit. The output is denoted by the characters S0-S7 and the letter "g" in the trash. The HNG gate is also used in the construction of the 4-bit ripple carry adder. A total of sixteen trash values are generated by the proposed adder, which incurs a quantum cost of forty-eight. Figure 7 depicts the reversible 8-bit ripple carry adder that was suggested before.

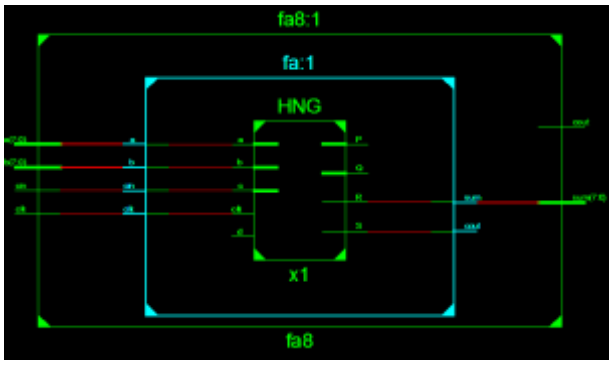


Figure 7: Proposed 8-Bit RCA using HNG Gate

**6.0 Design And Implementation**

Using the Xilinx ISE 14.5 tool, the design architectures are created in the VHDL programming language. The VHDL codes are simulated using the ISIM tool that is included in Xilinx, and the simulation results are then applied to the Spartan LX45 board for processing. Figures 8 illustrate the RTL design of an 8x8 Vedic multiplier.

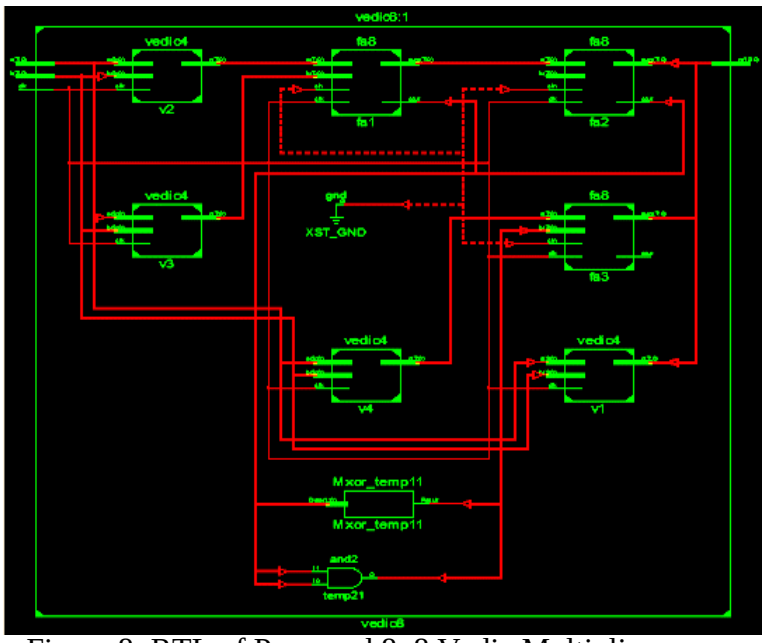


Figure 8: RTL of Proposed 8x8 Vedic Multiplier

The RTL description of a circuit, which stands for "Resister Transfer Level," details the registers of the circuit as well as the sequence of transfers that take place between the registers. However, the RTL description does not reveal the hardware that is utilized to perform these operations. It is used to decide the size of the registers as well as the number of registers that are utilized.

**2. Results And Discussion**

All the blocks are modeled using Verilog HDL. The simulation results of the proposed design are verified using Xilinx ISE ISim. This achieves functional verification of the conceptual design which enables the developer to synthesize ("compile") their designs, and perform timing analysis.


Figure 9: Simulation result of 8-bit RCA

Observations on the time delay and power consumption of proposed 8-bit reversible, nonreversible, and [8] adders were made, compared, and reported in Table 1.

Table 1. Time and Power Comparisons of proposedlogic

| **Parameters** | **IrreversibleRCA** | **Ref.[8]** | **Proposed ReversibleRCA** |
|---|---|---|---|
| Time Delay (ns) | 11.2 ns | 7.88 ns | 7.2 ns |
| Power (mw) | 0.047 | 0.0114 | 0.0101 |

The findings made above indicate that the reversible ripple carries adder that was presented is more time and power-efficient than the design that was proposed in [8], as well as irreversible logic.


Figure 10: Simulation Result of 8x8 Vedic Multiplier

Table 2 presents a comparison of the 8-bit reversible Vedic multiplier with the conventional multiplier (Booth), as well as the reversible multiplier [8], in terms of aspects such as time delay, power consumption, and space utilization.

Table 2. Comparison of Multiplier Designs.

| **Parameters** | **Conv.Booth Multiplier** | **Ref [8]** | **Proposed Multiplier** |
|---|---|---|---|
| Time Delay | 27.72ns | 21.44ns | 20.249ns |
| Power (mw) | 0.430mw | 0.299mw | 0.278mw |
| Area (no.slice LUTs.) | 171 | -- | 108 |

The proposed 8-bit reversible multiplier is more efficient and optimized than the conventional 8-bit booth multiplier and design proposed in [8]. The power dissipation, speed, and area utilization in terms of LUT are improved by 36.36%, 27.93%, and 35.6% respectively with respect to the conventional booth multiplier. Also proposed design has a 6.2 % power and 6 % speed improvement over the design [8]. The improvement in power dissipation is achieved by the 3*3

reversible gates, which are the fundamental blocks of the proposed design but in [8], Viswanath and Ponni utilized a 4*4 gate (TSG). The proposed Low Power Reversible Vedic multiplier and conventional booth structure are implemented using VHDL programming language, simulated and synthesized using Xilinx ISE 14.5, andget implemented using Spartan xc6slx45-2csg324 FPGA kit.

## 3. Conclusion

The power consumption and speed of operations of the suggested design are decreased as compared to the other design. This is because the fast, low power, and area-efficient reversible logic-based adder and Vedic multipliers with lower hardware complexity are incorporated. In the Vedic multiplier, having a lower total number of adders results in less wasted space and power while also speeding up the calculation process. The suggested logic is realized in the form of a program written in Verilog HDL, which is then simulated and synthesized with the help of the Xilinx ISE 14.5i software. As a result of the output that was synthesized, it was determined that the proposed method utilized approximately 36 percent less power, an area that was 37 percent less, and 26 percent higher performance when compared to the conventional circuit. Additionally, the proposed method utilized 5 percent of less power and 7 percent speed over.

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