ISSN 2063-5346

RECENT ADVANCES IN THE CHALLENGES OF ULTRA LOW-POWER DESIGNS FOR NEXT GENERATION WIRELESS DEVICES IN WIRELESS COMMUNICATION SYSTEMS USING VLSI DESIGN & EMBEDDED SYSTEM CONCEPTS

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Article History: Received: 10.05.2023 Revised: 29.05.2023 Accepted: 09.06.2023

Abstract

In this research article, we present some of the recent advancements in the challenges of ultra low-power designs for next generation wireless devices in wireless communication systems using VLSI concepts. The material presented in this paper could serve as a research guide for many of the researchers who want to work in this area.

Keywords : VLSI, Wireless, Device, Communication, Synthetic, RTL, Low Power, Design.

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DOI:10.48047/ecb/2023.12.9.117

1. Introduction Remarks

In this section, we present the details of the Components of Power, Energy & Time. The important parts which has to be taken care of in VLSI design are the E P T. The increasing demand for wireless communication and the need for energy-efficient solutions have led to the development of various techniques aimed at improving energy efficiency in wireless communication systems. This is particularly important in low-power applications where energy resources are scarce and operating costs need to be minimized.

Energy-efficient techniques focus on optimizing different aspects of wireless communication systems to reduce energy consumption while maintaining reliable communication. Some of the key techniques used in energy-efficient design include:

Power Management: Intelligent power management techniques are employed to optimize power usage in wireless devices. This includes adaptive power control, dynamic power allocation, and sleep modes to minimize energy consumption during idle periods.

Transmission Optimization: Efficient transmission schemes are designed to minimize energy consumption during data transmission. Techniques such as power adaptation, adaptive modulation, and coding schemes aim to transmit data using the minimum required power while maintaining the desired quality of service.

Energy Harvesting: Energy harvesting techniques, such as solar or kinetic energy harvesting, are utilized to supplement or replace battery power in low-power applications. This allows for longer operation times and reduced dependence on external power sources.

Network Optimization: Network-level optimizations are employed to reduce energy consumption in wireless networks. This includes techniques such as base station sleeping, load balancing, and resource allocation algorithms to ensure efficient use of network resources.

Protocol Design: Energy-efficient protocols, such as duty cycling and low-power listening, are designed to minimize energy consumption during communication by reducing unnecessary transmissions and maximizing the time spent in low-power sleep modes.

Hardware Optimization: Energy-efficient hardware designs, including low-power transceivers, power amplifiers, and energy-efficient signal processing algorithms, are developed to minimize energy consumption in wireless devices.

The advancement of energy-efficient techniques in wireless communication systems is crucial to meet the increasing demand for wireless communication while addressing the limitations of energy resources and operating costs. These techniques play a vital role in enabling sustainable and long-lasting wireless communication solutions in various applications, ranging from IoT devices to cellular networks., i.e., [13],

- Energy
- Power
- Time

2. Mathematical Model

The mathematical model is given by

$$E = \int C.V_{dd}^2.f_c + V_{dd}.\ I_{leak\ (dt)}$$

Therefore, the total power is given by

Total Power = Switching Power + Leakage Power

This study examines the most recent discoveries and advancements in the field of low-power VLSI design. Despite the fact that Low Power is a well-established area,

it has seen several advancements, including transistor sizing, process shrinkage, voltage scaling, clock gating, and adiabatic logic. Although there are other types of power consumption, dynamic power and leakage power are the two that have the most impact on CMOS circuits. The power utilised by a gadget when it is actively moving from one state to another is known as dynamic power [1].

Internal power (also known as short circuit power) is consumed internally to the device while it is changing state, and switching power is consumed while charging and discharging the loads on a device. The power spent by a device that is not related to state changes is known as leakage power. When a device is both static and switching, leakage power is consumed, however the main concern with leakage power is when the device is idle, as all the power consumed in this state is considered "squandered" power [1].

Reverse bias current, sub threshold channel leakage current, drain driven barrier lowering leakage, gate induced drain leakage, punch through, narrow width effect, gate oxide tunnelling current, and hot carrier injection current are some of the reasons of leakage power shown in Figs. 1 & 2 respectively. The aim of this essay is to discuss recent developments in low-power design. There are two schematic designs which are shown in the Figs. 1 & 2 respectively. Here, it gives the leakage current and the capacitance that could be designed in the form of a stray capacitance as shown [1].

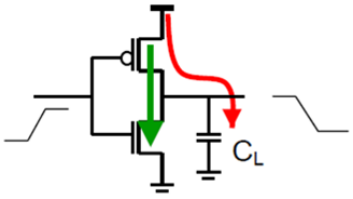

Fig. 1 : Schematic design - 1

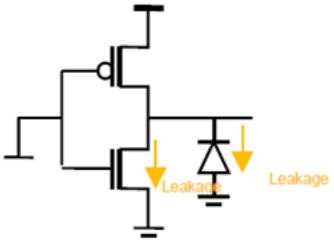

Fig. 2 : Schematic design – 2

- Reducing Switching Power:
- Reduce operating Voltage
- Lower Switching Capacitance
- Reduce Switching Frequency
- Reducing Leakage Power:
- Reduce operating Voltage
- Reduce number of leaking transistors

3. Power Consumption in a Mobile Phone

In this section, we present the power consumption in a mobile phone. The concepts that are to be used are as given below in the form of a graph as shown in Fig. 3. Previously, the primary concerns of VLSI designers were area, performance, cost, and reliability; power was usually only a secondary factor. In recent years, there has been a shift in the design considerations for electronic devices, where power consumption has gained equal importance alongside area and speed factors. This shift has been driven by various factors, with the notable success and proliferation of personal computing devices and wireless communication systems playing a significant role. The increasing popularity of portable desktops, audio and video multimedia products, and wireless communication devices such as personal digital assistants and personal communicators has created a demand for high-speed computation and complex functionality with low energy consumption. These devices are designed to be compact, lightweight, and energy-efficient to cater to the needs of modern consumers who rely on

mobile computing and communication capabilities.

This demand for energy-efficient devices has influenced the design priorities of manufacturers and researchers. Power consumption has become a critical consideration in the development of new technologies and systems. Achieving high-performance computing and advanced functionality while minimizing energy consumption has become a key challenge.

To address this challenge, significant efforts have been made in developing energy-efficient hardware architectures, low-power circuit designs, and power management techniques. These advancements aim to optimize power usage, reduce leakage currents, and enable dynamic power scaling to meet the energy requirements of modern computing and communication devices.

The shift towards giving equal weight to power, area, and speed factors in design decisions reflects the growing awareness of the need for sustainable and energy-efficient solutions. It acknowledges the importance of minimizing power consumption to prolong battery life, reduce environmental impact, and enable the widespread adoption of electronic devices in various domains. Overall, the increasing demand for high-speed computation and complex functionality with low energy consumption, driven by the success of personal computing and wireless communication systems, has played a significant role in the shift towards considering power as a crucial design factor in electronic devices.

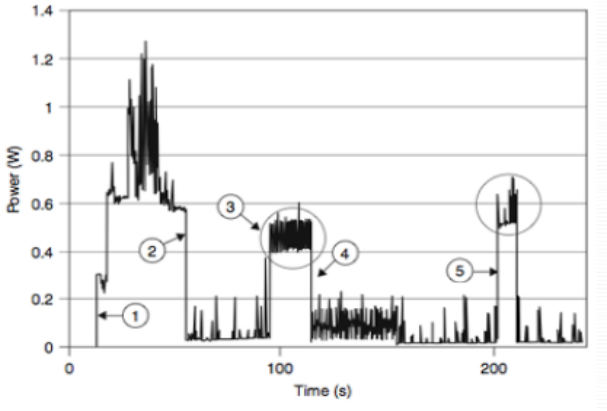

Fig. 3 : How to reduce the power consumption in a typical mobile phone

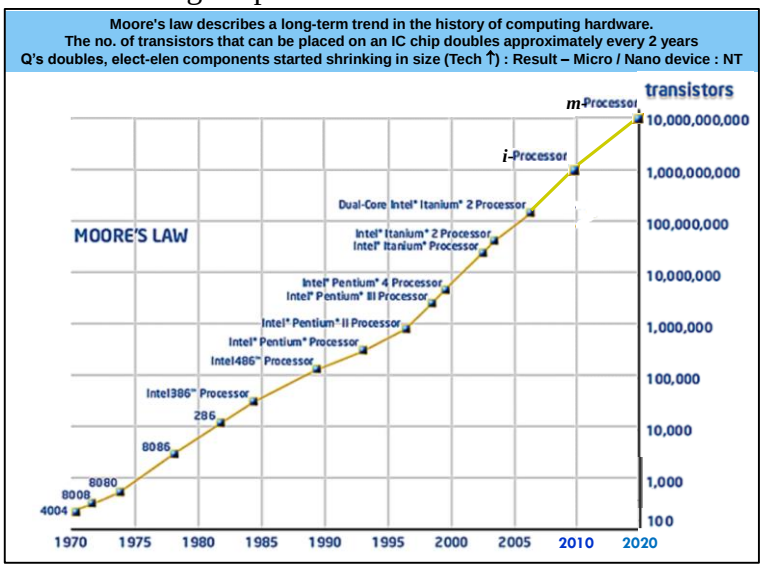

Fig. 4 : Moore's law is a concept that outlines a consistent pattern in the development of computing hardware. According to this law, the number of transistors that can be integrated onto an integrated circuit (IC) chip roughly doubles every two years. This exponential growth in transistor count has led to significant advancements in technology, as electronic components have been able to shrink in size. As a result, we now have micro and nano devices that have revolutionized various fields.

- Power is turned on, and the keypad and LCD backlights are activated, welcoming the user.
- The keypad backlights turn off, causing the display to go dark.
- The display is turned on, but the keypad backlights remain off.
- The display goes blank, indicating no active content is being shown.
- When the flip is closed, the external display backlight is turned on.

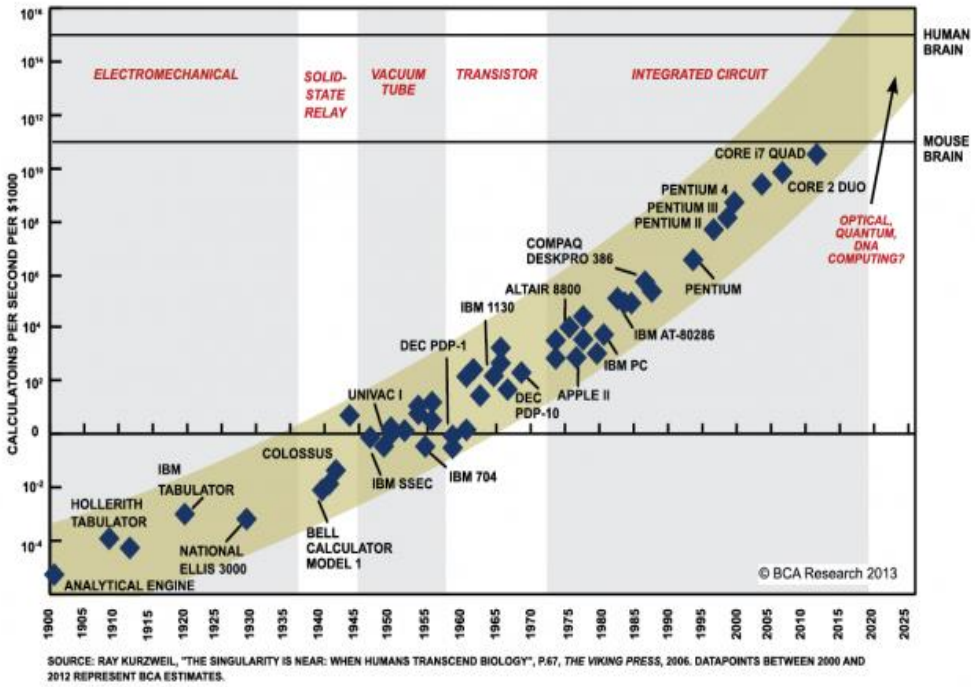

Fig. 5 : Moore's law characterizes a long-standing trend in the evolution of computing hardware, wherein the number of transistors that can be accommodated on an integrated circuit (IC) chip approximately doubles every two years. This remarkable growth in transistor density has facilitated a corresponding increase in computational power, as electronic components have steadily decreased in size. Consequently, this technological advancement has led to the development of micro and nano devices, which have revolutionized numerous fields and applications.

3. Mobile Phone Power Consumption @ 90nm

In this section, we present the mobile phone power consumptions at a level of 90 nano meter [2].

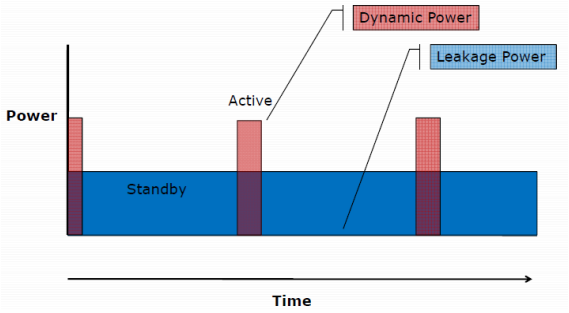

Fig. 6 : Plot of dynamic power vs the leakage powers

Table 1 : Intel measured smart phone power consumpiton using identical display brightness

Intel Measured Smartphone Power Consumption (Identical Display Brightness)				
	Standby (3G)	Talk (3G)	Browsing (3G)	Video Playback 720p
Apple iPhone 4S	~38mW	~800mW	~1.3W	**~500mW**
Intel Medfield Reference	**~18mW**	~700mW	**~1.0W**	~850mW
Samsung Galaxy S II	~19mW	**~675mW**	~1.2W	~650mW

4. Real life power consumption numbers

In this section, we present some of the real life power consumption numbers in the form of a table as shown in table 1. The i.MX 7ULP processor series is NXP's most recent breakthrough in Ultra-Low-Power processing for applications that require long battery life. The i.MX 7ULP processor family is aimed at the increasing portable device market and includes NXP's sophisticated implementation of the Arm® Cortex®-A7 core, the Arm Cortex-M4 core, as well as 3D and 2D Graphics Processing Units (GPUs). The i.MX 7ULP family has a 32-bit LPDDR2/LPDDR3 memory interface as well as a variety of additional interfaces for attaching peripherals like WLAN, Bluetooth®, GPS, displays, and camera sensors [3].

5. Mainstream Low Power Techniques

In this section, we present the main stream low power techniques that could be used in the course of the VLSI designs as shown in the Fig. 5 [4][5].

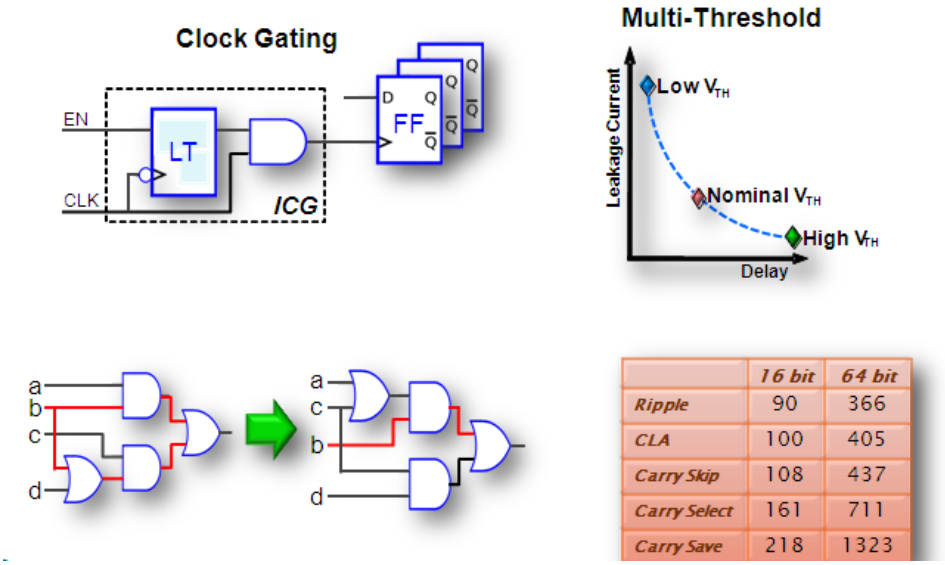

Fig. 7 : Plot of main stream low power frequencies with the schematic clock gating designs for 16 bit & 64 bit VLSI circuitries

6. Gate-level Power Optimization & Architectural Optimization with Advanced Low Power Techniques

In this section, we present the gate-level power optimization & architectural optimization with advanced low power techniques in the form of some diagrammatic representations as shown in the Fig. 6. Power dissipation has become an important characteristic in low power VLSI circuit designs as a result of the increased use of portable electronic devices and the evaluation of microelectronic technology. The circuit complexity and fast speed of evolving VLSI technology imply a large increase in power consumption. The energy dissipation in low-power CMOS VLSI circuits is generated by the charging and discharging of internal node capacitances owing to transition activity, which is one of the key variables that affects dynamic power dissipation. The optimization of design techniques at all stages is required to reduce power, area, and enhance speed [15].

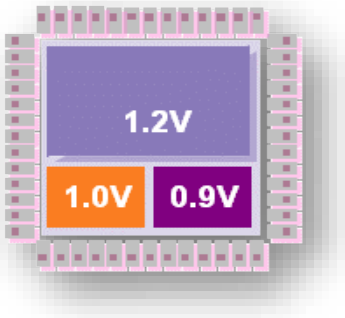

Fig. 8 : Multi voltage levels (MV)

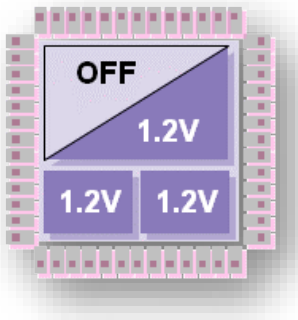

Fig. 9 : MTC MoS power gating during shutdown levels

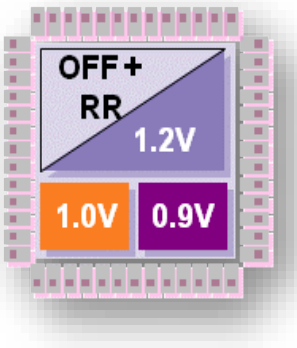

Fig. 10 : MV and power gatings

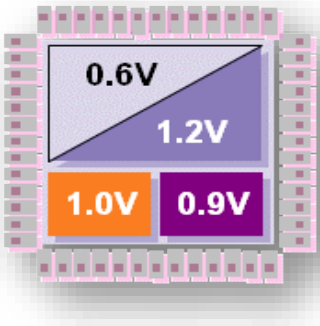

Fig. 11 : Low VDD standby

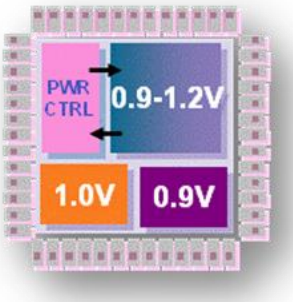

Fig. 12 : Prototype

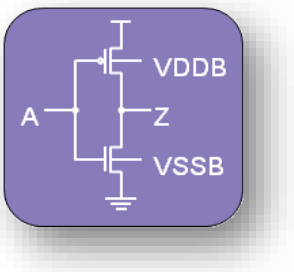

Fig. 13 : Dynamic or adaptive

7. Well Biasing

In this section, we present the well biasing concepts such as the Voltage & Frequency Scaling (VTCMOS) - (DVS, DVFS, AVS, AVFS) [7]

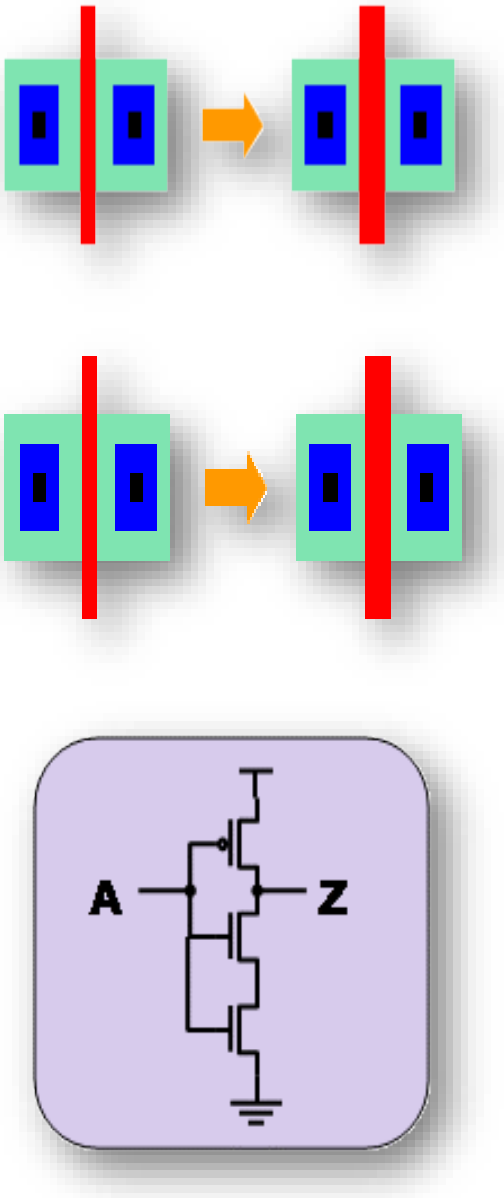

Fig. 13 : Stack effects circuit diagrams

8. Power Gating

In this section, we present some of the power gating concepts that could be used in the VLSI design using the cadence tools at a very low nano meter level [6].

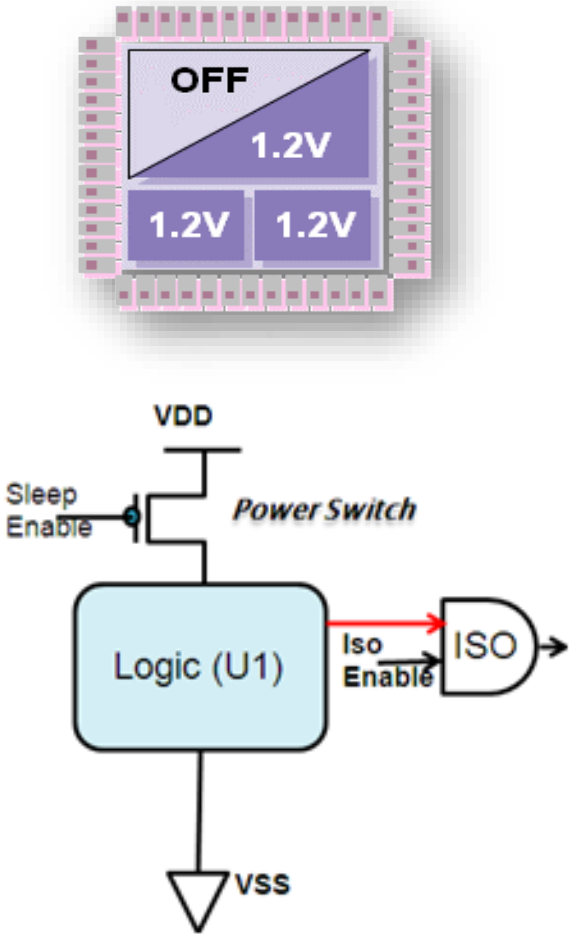

Fig. 14 : Switch off in-active blocks

- Reboot or reset the blocks on wakeup
- Isolate outputs to protect ON regions from corruption
- Incurs shutdown and wakeup cycles

9. Multi-Voltage

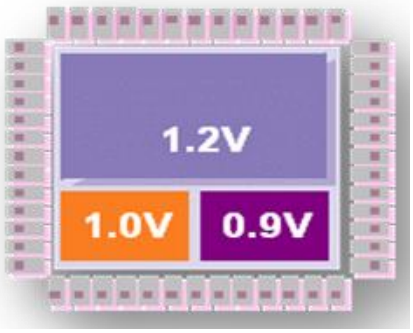

Fig. 15 : Multi voltage level block chip set design.

Here, we present the different blocks operate at different voltages, depending on performance needs - Only timing critical blocks need to operate at higher voltage, i.e., the interfaces between different voltage levels need to be managed [8]

10. Choosing the logic to be switched off

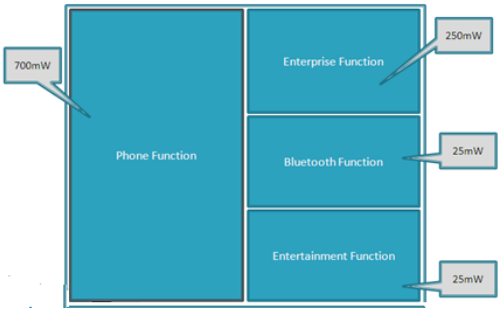

Fig. 16 : Schematic Diagram

The complexity and speed of circuits increase as VLSI technology progresses, resulting in significant power consumption. Small size and great performance are two opposing restrictions in VLSI design. The activities of the integrated circuit (IC) designer have been involved in the trading of these restrictions. There are numerous design issues, and power efficiency has become increasingly crucial as a result. The most portable systems in use today, which are powered by batteries, are capable of doing jobs that need a large number of calculations. The most significant feature of Moore's Law is that it has become a universal forecast of semiconductor industry growth. According to Moore's law, the number of devices in a chip doubles every 18 months. This will result in a greater number of transistors being utilised [15].

11. Summary of Low Power Impact on Design Flow

Table 2 : Comparision b/w power v/s design complexities

Low Power Technique Used	Dynamic Power Reduction	Static Power Reduction	Timing & Area Penalty	Verification Impact	Implementation Impact
Clock Gating	Moderate	None	Minimal	Minimal	Minimal
Multi-Vt Optimization	None	Moderate	None	None	Minimal
Multiple Voltage Islands	High	Moderate	Minimal	High	Moderate
Power Gating	Minimal	Very high	Very high	Very high	Very high
Biasing: Standby / Active Leakage	None	Minimal / Moderate	Minimal	High	High
Voltage & Frequency Scaling	Very high	Moderate	Very high	Very high	Very high

12. Basic Concept of Power Intent

There is also a lot of pressure on high-end goods manufacturers to lower their power use. At 100-200 MHz clock rates, modern performance enhanced microprocessors dissipate as much as 15-30 W. It may be projected that a 10 cm2 microprocessor clocked at 500 MHz (a reasonable estimate

for the next decade) will require around 300 W in the future. The expense of packaging and cooling such devices is prohibitively expensive. Because core power consumption must be dissipated through the packaging, as chip power consumption rises, more expensive packaging and cooling solutions are necessary. As a result, lowering the power consumed in high-performance systems has a clear cost benefit [14].

- Starting with your functional design…
- Can some logic run at lower voltage?
- Can some logic be turned off when not in use?
- Does the state of that logic need to be preserved during shutdown?
- What protection is required between these?

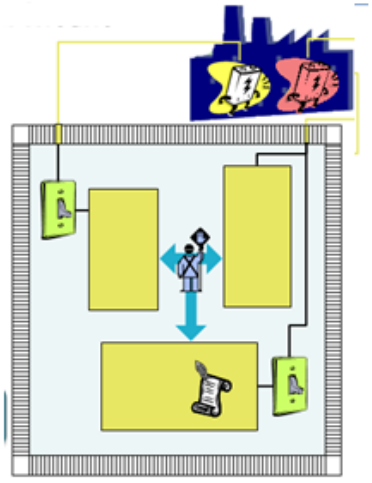

Fig. 17 : Power behaviour interpretations during design process

This power behavior defines your power intent what we are going to use in the design of VLSI circuits for wireless applications [7][8].

13. Functional Intent vs. Power Intent What is the difference?

In this section, we present the functional intents versus the power intents w.r.t. what is the main difference in the form of a table as shown. Average power consumption is a major design consideration in these applications. When using off-the-shelf components that aren't tuned for low-power operation, the predicted power budget for a battery-powered, A4 format, portable multimedia terminal is around 40 W. This terminal would require an unacceptable 6 kilos of batteries for 10 hours of operation between recharges, despite advanced Nickel-Metal-Hydride (secondary) battery technologies giving roughly 65 watt-hours/kilogram. Even with new battery technologies like rechargeable lithium ion or lithium polymer cells, battery lifetime is estimated to improve to around 90-110 watt-hours/kilogram over the next 5 years, resulting in an unsatisfactory 3.6-4.4 kilos of battery cells. Current and future portable devices will suffer from short battery life if low-power design strategies are not used [14].

Table 3 : Comparison

Functional intent specifies	Power intent specifies
Architecture Design hierarchy Data path Custom blocks Application State machines Combinatorial logic I/Os EX: CPU, DSP, Cache Usage of IP	Power distribution architecture Power domains Supply rails Shutdown control Power strategy Power state tables Operating voltages Usage of special cells Isolation cells, Level shifters Power switches

Industry-standard interfaces Memories etc	Retention registers
Captured in RTL	Captured in UPF

14. Advanced low power techniques require special cells

Designed to protect interfaces between power domains (isolation cells, level shifters) and/or implement new power behavior (switches, retention cells, always-on logic). This is also referred to as the "power management cells" [9][10].

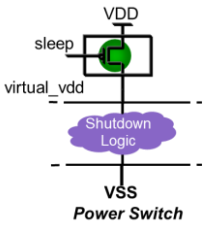

Fig. 18 : Power switch design

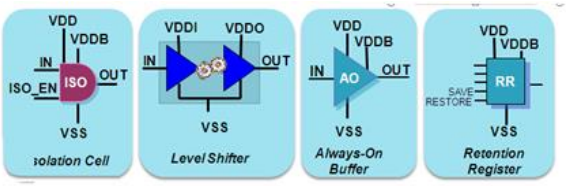

Fig. 19 : Pictorial representation of a isolation cell, level shifter, always on buffer & a retention register

15. Conclusions

In this research paper, the authors have presented a Recent advances in the challenges of ultra-low-power designs for next generation wireless devices in wireless communication systems using VLSI concepts.

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