Seventeen Multilevel Inverter With Low Total Harmonic DistortionBy Using Switching Power Semiconductor Devices

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ABSTRACT: This Paper is related to efficient conversion and flexible control of power using fast switching power semiconductor devices. Flexible control of power has urged the need for power electronic converters in technological development due to several factors, the most important being the ever-increasing compactness, efficiency, reliability, ease and speed of the semiconductor devices and the deployment of Digital Logic Circuits (DLC), Digital Signal Processors (DSP), Programmable Logic Controllers (PLC), microprocessor/microcontroller in power converters. However, power converters inflict severe complications on power quality. Increased dependency on power converters and the need to provide quality power has mandated that all such power electronic systems should have less Total Harmonic Distortion (THD) and improved input power factor. This Paper gives a brief overview of the basic topologies, modulation strategies, applications and common issues encountered in Multilevel Inverters (MLI). A brief review of the hybrid topologies is also presented followed by the description of power circuit, switching states, working and hardware prototype of the cascaded hybrid MLI topology considered in this Paper.

KEY WORDS : THD, PWM , ADOP.

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1. INTRODUCTION

1.1STATE OF THE ART OF MULTILEVEL INVERTERS

DC/AC converter is also called as inverter. It converts a stiff input voltage/current into a three phase AC output voltage/current with variable magnitude and frequency. The traditional 3 phase, 2-level inverter comprises of six switches, hence called as six switches or six pulse inverters[1]. It produces output line voltage or current with maximum of two levels either 0 or $\pm V_{DC}$ / I_{DC}. The major drawback of traditional 3 phase, 2-level inverter is that the output voltage contains high ripple, produce high dv/dt, increasing the stress on the switches and switching loss[2]. To overcome the drawback of the traditional 3, 2-level inverter, Neutral Point Clamped (NPC) inverter was introduced by Nabae that paved the way for multilevel

inverters. It eliminates the need of step-up transformers, reduces the harmonic content, capable of scaling up the voltage and power rating is the intriguing features of MLI[3]. It accumulates the output voltage in layers employing different Pulse Width Modulation (PWM) techniques which vertically slices the modulating reference signal to produce similar output.

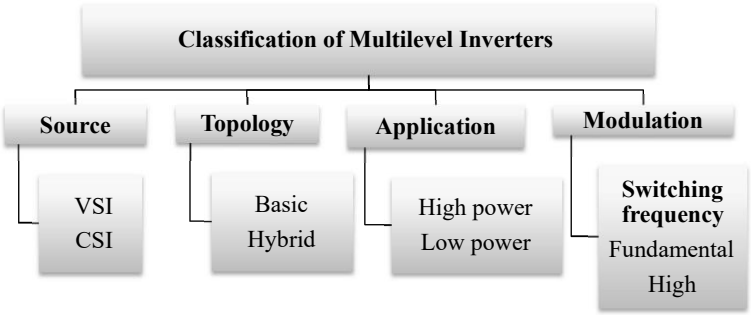

Figure 1.1 Classifications of Multilevel Inverters

MLI has been receiving greater attention in current era due to its attractive features such as low dv/dt, negligible electromagnetic interference, lower THD and stress on power devices thus providing cost effective solution for industrial applications. Figure 1.1 illustrates the broad classification of MLI[4].

1.2 Review of Basic Multilevel Inverter Topologies

Figure 1.2 lists the most basic MLI topologies widely used. The first three-level inverter was proposed by Nabae (1980) called Diode Clamped Multilevel Inverter (DC-MLI) which is also referred as Neutral point clamped inverter. This topology works efficiently when operated at fundamental switching frequency and is popularly used in motor drive applications[5]. The major drawback of DC-MLI is the proportional increase of clamping diodes and capacitor voltage balancing with increase in level which makes it bulky and requires complex control. Hence higher level DC-MLI is seldom used in industries. The 3, 5-level DC-MLI is shown in Figure 1.3[6].

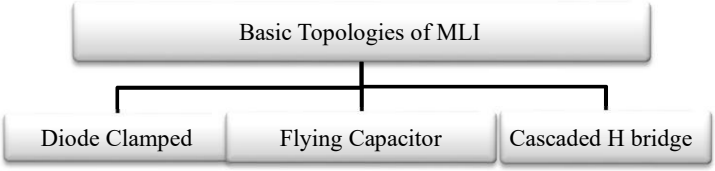

Figure 1.2 Basic Multilevel Inverter Topologies

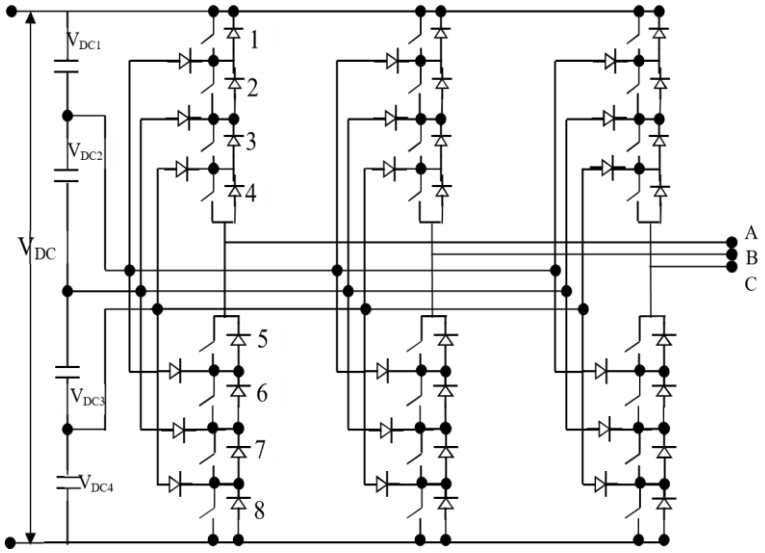

Figure 1.3 Topology of 3 phase, 5-level DC-MLI

As an alternative a new topology called the Flying Capacitor Multilevel Inverter (FC-MLI) was introduced in 1992 by Meynard & Foch[7]. The structure of 3phase, 5-level FC-MLI shown in Figure 1.4 differs from DC-MLI by replacing the clamping diodes by laddered DC bus capacitors. FC-MLI also has its limitation similar to DC-MLI, when extended to higher levels increasing the cost and size drastically. In addition, it requires several DC capacitor banks with separate pre-charge circuits for inverter initialization and complex voltage balancing circuits which complicates the modulation process and hinders the performance of the inverter during ride through conditions[8].

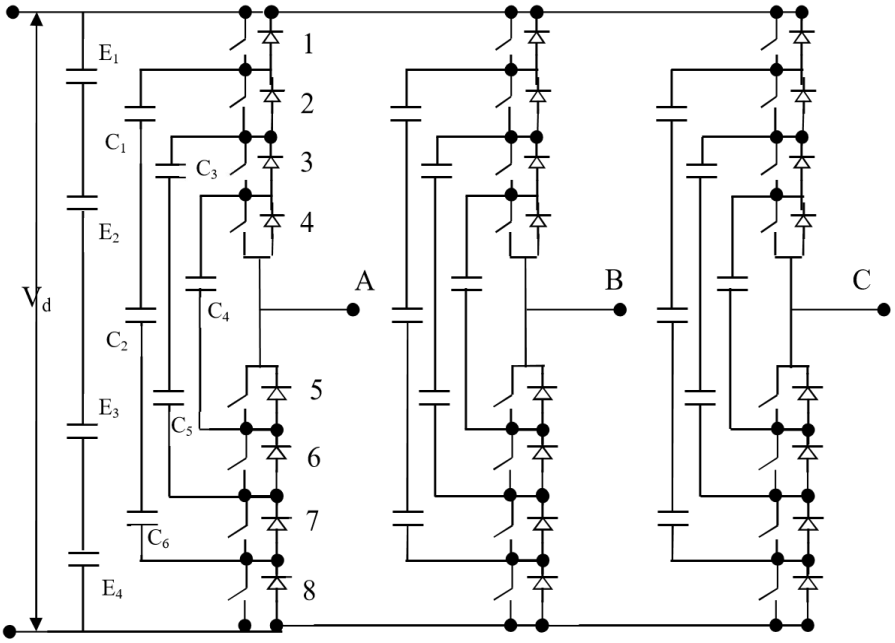

Figure 1.4 Topology of 3 phase, 5-level FC-MLI

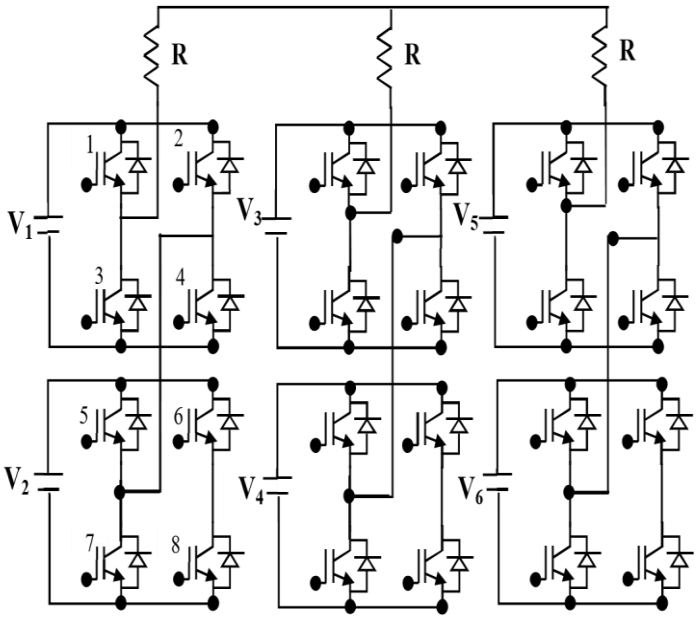

Figure 1.5 Topology of 3phase, 5-level CHB -MLI

The disadvantage of both DC-MLI and FC-MLI was overcome by a new topology called Cascaded H-Bridge Multilevel Inverter (CHB-MLI) after mid 1990's (Lai &Peng 1996). The advantage of this topology is that it does not require clamping diodes and capacitors. The modular structure of 3phase, 5-level CHB-MLI as shown in Figure 1.5, comprises of identical power modules connected in series which provides a cost effective solution and ease of increasing the voltage and power rating of the MLI (Hammond 1997). A comparison of 3, 5-level basic MLI topologies based on its structure and component count is listed in Table 1.1. It can be observed from the table that CHB-MLI is advantageous as the usage of clamping diodes and capacitors are eliminated and the requirement of DC bus capacitor is reduced to half. Contrarily it requires six isolated DC sources. CHB-MLI is highly recommended for hybrid electric vehicle applications due to ease of regulation and modular structure.

Table 1.1 Comparison of Basic MLI topologies

Topology	**DC-MLI**	**FC-MLI**	**CHB-MLI**
No of Main Switches	24	24	24
No of Free Wheeling Diode	24	24	24
No of Clamping diodes	36	0	0

No of Balancing Capacitors	0	18	0
No of DC bus Capacitors	12	12	6
No of DC source	1	1	6

1.3 Review of Modulation Strategies for Multilevel Inverters

The control of output voltage is mandatory in industrial applications to compensate the input voltage variation and for regulation of inverters for which internal inverter control called pulse width modulation is mostly preferred[9]. The process of switching a semiconductor device using electronic circuit from one state to the other is termed as Pulse width modulation. The first modulation technique was developed in mid-1960s by Kirnnich, Heinrick, and Bowes.Each technique is characterized based on the switching frequency, modulation index (m_a), speed of response, losses and total harmonic distortion (Rashid 2001)[10]. PWM techniques for MLI based on the switching frequency are classified as shown in Figure 1.6. Low and high switching frequencies correspond to commutation of the device either twice or several times in a switching period respectively[11].

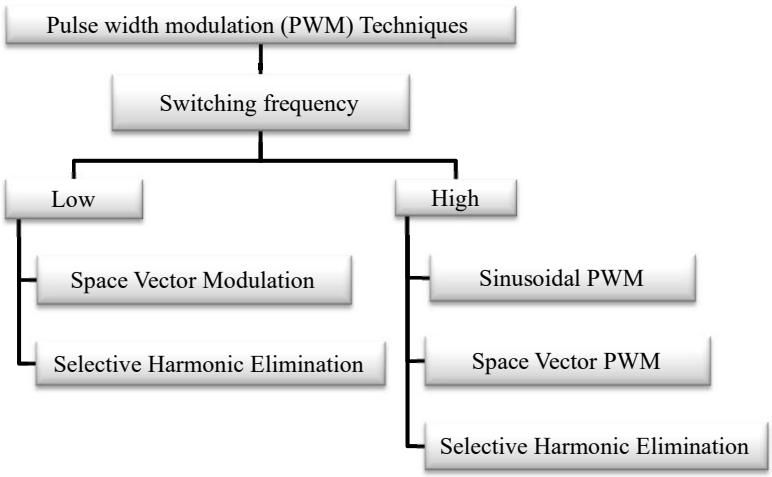

Figure 1.6 Classification of Modulation Techniques

Low power converters typically operate at high switching frequencies ranging between 5 kHz to 25 kHz (Bin Wu 2006) due to reduced THD. Various PWM schemes have been developed and analysed (Tolbert & Habetla 1999, Veenstra & Rufer 2005) so as to control the fundamental voltage and to eliminate certain lower order harmonics, via control of pulse width. Hence in this thesis conventional high switching frequency technique namely Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are considered[12]. A brief overview of the recent advancements of SPWM and SVPWM is presented. Sinusoidal pulse width modulation was introduced by Schonung & Stemmler

(1964), Lee & Sun (1988)[13]. It is also called as sub harmonic oscillation technique. SPWM basically compares three phase sinusoidal modulating reference (V_{REF}) at fundamental frequency with high frequency triangular carrier to trigger the switches of the inverter. For an N-level MLI, (N-1) high frequency carriers are used hence it is termed as Multicarrier Sinusoidal Pulse Width Modulation (MCSPWM)[14]. In MCSPWM the switches are triggered by comparing the (N-1) carriers with the modulating reference. A major contribution to the classification of several modulation possibilities based on the carrier disposition process by Carrara set the stage for different SPWM modulation techniques as listed in Figure 1.7[15].

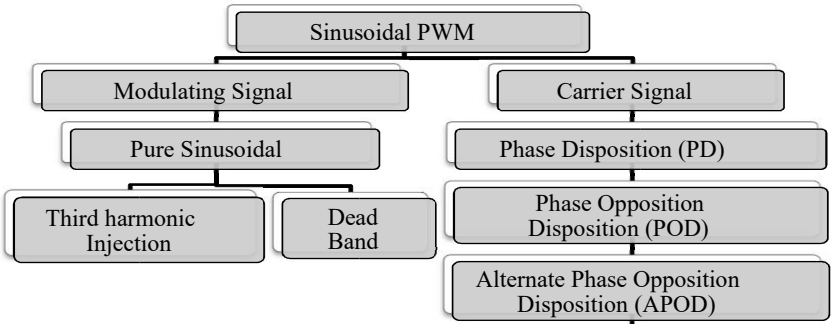

Figure 1.7 Multicarrier Sinusoidal PWM Techniques for MLI

Based on vertical and horizontal distributions of triangular carrier MCSPWM are classified into Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) (Carrara et al. 1992)[16]. In APOD carrier distribution is vertical while Hybrid (Hyb) and Phase Shift (PS) belong to horizontal distribution of carriers. Considering the THD of output line voltage and switching loss PD is preferred as best choice due to the asymmetry around the time axis which in turn improves the harmonic spectrum of the line voltage (Massoud et al. 2003) PS-PWM is generally preferred for FC-MLI and CHB-MLI and PD-PWM for DC-MLI[17].

1.4 Classification of MLI based on Source

Depending on the type of input DC source MLI can be classified into voltage and current source inverters. The structure of 3phase Voltage Source Inverter (VSI) and Current Source Inverter (CSI) differs from each other only by the connection of diodes and load. In VSI, IGBT switches with antiparallel diode are used and the output is directly connected to the motor terminals[18]. Whereas in CSI, IGBT switches with series diode are employed and the output is linked to capacitor filters and load. Current Source Multilevel Inverter (CSMLI) are widely used in high power drive applications than Voltage Source Multilevel Inverter (VSMLI) due to its inherent four quadrant operation while VSMLI is used in both high and low power

applications. To increase the voltage and current rating of the inverter, modules are cascaded in VSI and paralleled in CSI[19].

1.5 REVIEW OF RECENT HYBRID MLI TOPOLOGIES

The first innovative medium voltage PWM inverter topology proposed for adjustable speed drive application comprises of three standard 3-phase inverter modules interconnected through inductors. It was widely used in VAR compensation and variable speed drive application. A new type of inverter called Mixed Level-Hybrid Multilevel Inverters (ML-HMLI) for high-voltage high-power application was introduced to reduce the requirement of separate DC sources. It is achieved by replacing the H bridge cell of CHB-MLI by DC-MLI or FC-MLI[20]. Due to size and ability of switched capacitors to operate at high switching frequencies, switched capacitor technique was introduced for multilevel inverters. Switched capacitor circuits and their control becomes complex when the difference between input and output voltage increases (Luo & Ye 1999). To overcome the disadvantage of switched capacitor technique, switched inductor technique was proposed for multilevel inverters (Luo & Ye 2000).

Table 1.2 Comparison of commercial 4- Level Multilevel Topologies

Topology	No of Dc link Capacitor + auxiliary Capacitor	No of Clamping Diode	No of Switches	No of DC source
3-phase (DC-MLI)	3 + 0	36	18	1
3-phase (FC-MLI)	3 + 18	-	18	1
3-phase CHMLI	**-**	**-**	**18**	**4**

1.6 PROBLEM STATEMENT AND OBJECTIVE OF THE PAPER

1. In high-power photovoltaic (PV) systems, conventional multi-level inverter (MLI) topologies have drawbacks such as significant total harmonic distortion (THD) and the requirement of several switching components as seen from the Table 1.2, which raises the overall cost.

2. The size and price of the inverter rise even if adding a large filter element to the input side may greatly decrease THD. Thus, achieving pure sinusoidal AC output with low THD is a major challenge for conventional MLIs.

3. A proposed MLI addresses these issues by modifying the cascaded H-Bridge structure and using Alternate phase opposition disposition (APOD) PWM technique to decrease THD at the output.

4. The suggested inverter does not need any extra voltage balancing capacitors or clamping diodes since it contains 6 unidirectional switches and 2 bidirectional switches. For the purpose of producing gate pulses, the switching states and APOD PWM operation are thoroughly discussed.

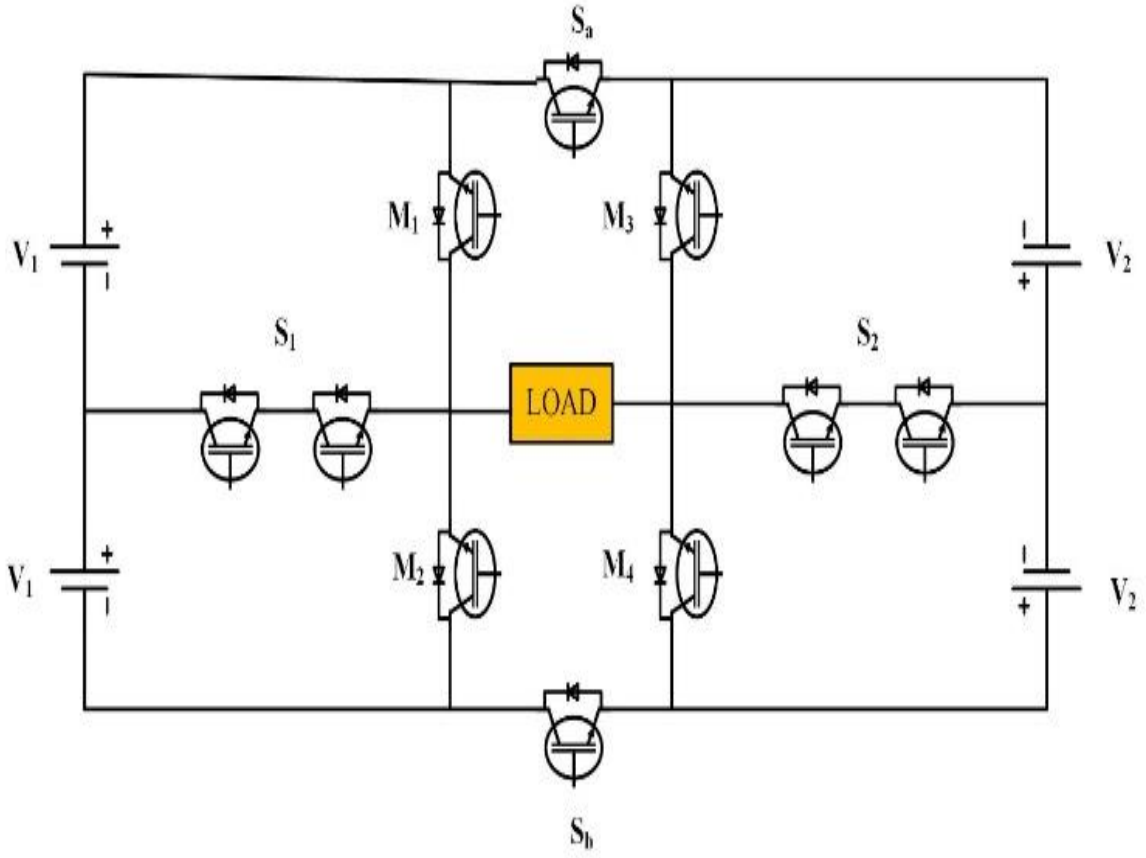

Figure 2.2. Proposed MLI Topology

2. Results: In Simulink/MATLAB, an FFT analysis is performed to find the overall harmonic distortion on the frequency spectrum (see Figures 38 and 39). Total harmonic distortion is a useful approach for dissecting any nonlinear conduct of a framework.Typically, the fast Fourier transform (FFT) is used.The measured signal is converted from time domain to frequency domain. An FFT spectrum with the response can be used to display the changing information.The magnitude of the signal is shown against its frequency. 39th FigureThe FFT spectrum of a 17-level MLI is shown.

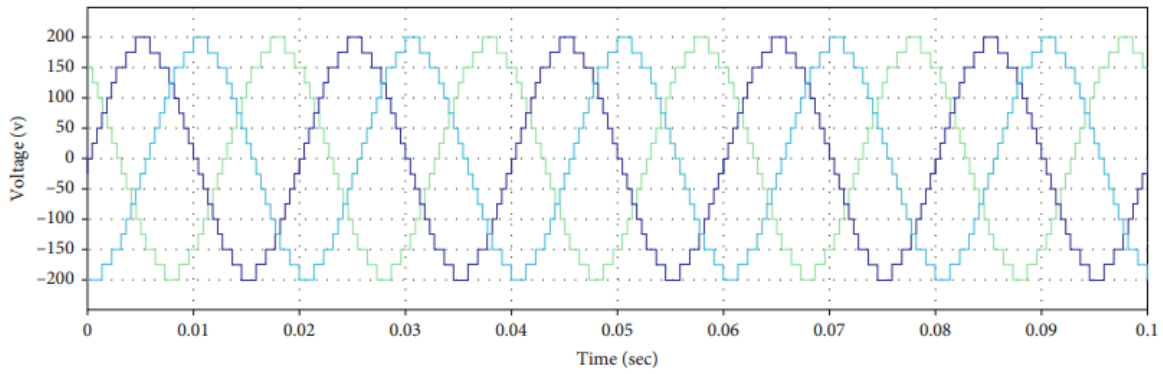

Figure : 3-phase MLI output.

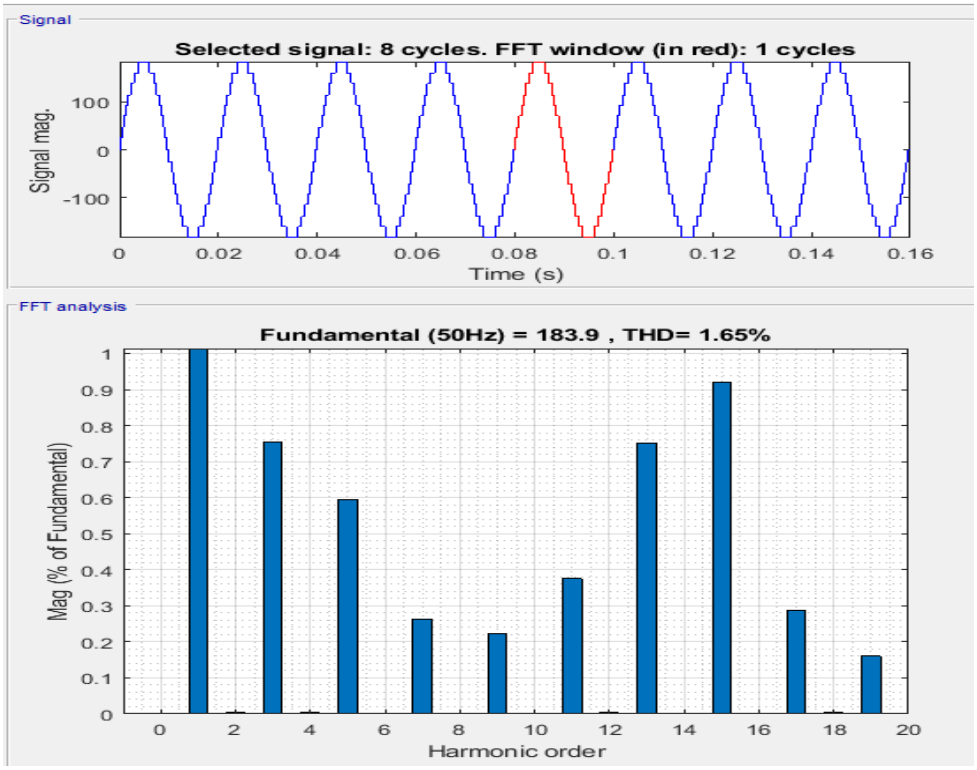

Figure 4. Voltage & THD obtained during traditional PWM method The Total Harmonic Distortion obtained during this method is 1.65 % which is shown in Figure 4.

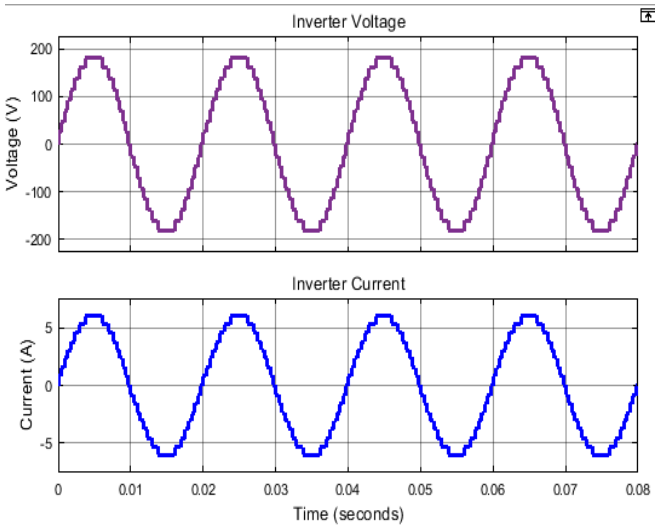

Figure 5. Voltage & Current Waveform with PWM technique for R load

Conclusion: The switching pattern of a multilevel inverter, where different switching modes are assigned specific patterns denoted by letters (A to R). The table provides information about the states of various switches (Sa, Sb, SY, S2, M4, M3, M2, M1) and the resulting output voltage (Vout) for each mode. Each mode represents a unique combination of switch states, and the table lists the corresponding states of each switch for all the modes. The switches Sa and Sb, as well as SY and S2, are auxiliary switches that play a role in controlling the output voltage waveform. The output voltage is determined by the combination of switch states in each mode, and the table includes the equation representing the output voltage for each mode. The values V1 and V2 represent specific voltage levels associated with the multilevel inverter. By analyzing the table, one can observe the patterns of switch states required to achieve different output voltage levels and waveforms. Each mode represents a specific configuration of the switches, and the corresponding output voltage equation provides insight into the resulting voltage waveform. Understanding the switching pattern in the table is crucial for designing and implementing control strategies for multilevel inverters. By selecting the appropriate mode and configuring the switches accordingly, the desired output voltage characteristics can be achieved. It is important to note that the values and equations in the table are specific to the multilevel inverter being analyzed. The switching pattern may vary depending on the specific design and requirements of the inverter. Overall, the table provides a comprehensive overview of the switching pattern of a multilevel inverter, illustrating the states of various switches and their impact on the output voltage. By studying the patterns and corresponding equations, one can gain insights into the operation and control of multilevel inverters, enabling the design of effective and efficient power conversion systems.

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