Section A-Research paper

Study on Transformer less Single Phase Grid Tied Inverter for PV Application

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Abstract:-

Multilevel inverters have gained significant attention in recent years due to their ability to generate high-quality output waveforms with reduced harmonics. The carrier-based PWM technique is widely employed to control the switching of power devices in multilevel inverters. This paper proposes a single phase multi-level inverter that uses the carrier base PWM techniques, summarizes the key concepts, advantages, challenges. The behaviour of the grid tied inverter while delivering a tightly controlled current is injected to the grid is studied in this work.

Introduction

Transformer-less inverters are becoming more widespread in grid-connected distributed generation (DG) systems in commercial and residential solar applications. This report uses a common-ground transformerless grid-tied inverter. The inverter shown uses a switched capacitor module (SC), a virtual DC connection, and the ability to double the boosting factor in one step. This grid-connected transformer-less architecture provides a five-level waveform at the output voltage terminal, which reduces harmonic distortion, dv/dt, and output filter size and cost.

Peak current controller (PCC) method and a tiny inductor-based filter are used to precisely control injected current to provide grid active and reactive powers with a rapid and robust dynamic response. As the PV panel is the input voltage source of the grid tied inverter, MPPT unit along with the peak current controller (PCC) block are the two main blocks of the control system. A filter based PLL system such as enhanced PLL (EPLL) as the synchronous unit is used for detecting the appropriate amplitude and phase of the local grid to have an adequately fast and robust dynamic response for the injected current. The measured grid current will be compared with the reference current waveform provided by the MPPT and PLL units within a sampling time and accordingly gate triggered pulses for the switches will be generated. The behaviour of the grid tied inverter while delivering a tightly controlled injected current to the grid will be studied.

Literature review

Grid-tied inverters are essential to distributed generation systems because they connect renewable energy sources to utilities. Due to their superior efficiency, lower cost, smaller size, and weight, transformer-less inverters for low-voltage single-phase grid-tied PV systems are becoming more popular. Also there has been reduction in the cost of PV modules. Due to this rise, typical PV power converters have evolved from single-phase grid-tied inverters to more sophisticated topologies to boost efficiency, power extraction from the sun, and dependability without increasing cost. [1] Presents an overview of PV energy conversion systems, including PV plant system configurations and PV converter topologies used in grid-connected systems. However there is an issue of leakage current for such type of inverters which depends on the topology structure and modulation scheme, have to be addressed very carefully [2].

In single phase grid tied PV system as presented in [3] it is actually possible to remove the transformer in the inverter in order to reduce losses, cost and size. Galvanic connection of the grid and the DC sources in transformer less systems can introduce additional leakage currents such as common mode leakage current because of

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the earth parasitic capacitance which has many demerits. This current increases utility grid harmonics, conducted and radiated electromagnetic emissions, and system losses. To eliminate the common mode leakage current in the transformer less photo voltaic grid connected system, an improved single phase inverter topology is presented in [4]. The improved Transformer-less inverters can tolerate the same low input voltage as full-bridge inverters and guarantee to eliminate common mode leakage current.

In order to eliminate the common mode (CM) leakage current in the transformer less photovoltaic (PV) system the concept of the virtual DC bus can also be utilised which is proposed in [5] [6]. By connecting the grid neutral line directly to the DC bus negative, stray capacitance between PV panel and ground is avoided. This eliminates the CM ground leakage current. The virtual DC bus generates negative voltage for negative AC grid current generation [7]. Thus, the whole bridge inverter's DC bus voltage is still needed. This concept yields a transformer-less inverter topology that uses switched capacitor technology to create a virtual DC bus.

The PLL is a simple yet effective tool with a nonlinear structure that can synthesize a signal whose phase angle is locked to that of a given input signal. In the proposed topology, a phase locked loop (PLL) is used to detect the appropriate amplitude and phase of the local grid. Although the basic PLL has been quite successful in addressing signal processing requirements for the communication systems, it suffers from two problems that hinder the use of this PLL for power system and control system applications: (1) the loop has a double frequency ripple even in the most ideal case where the input signal is a pure sinusoid, (2) The output signal magnitude has no relationship with that of the input signal. An enhanced PLL (EPLL) has been proposed in [8] & [10] to overcome the afore-mentioned problems of the PLL. The EPLL has successfully been applied to address several power electronics, power quality and power system problems.

By analyzing the instantaneous voltage supplied to the filter inductor, the publications [11] [15] give filter design guidelines for single-phase grid-connected PV inverters. Thus, precise filter inductance design guarantees switching ripple current under the target value. Power industry voltage source inverters convert DC voltage to AC voltage. DC conversion introduces harmonics in inverter output voltage. Variations in DC voltages and inverter switching angles affect the THD of inverter output voltage, which measures harmonic pollution in the power system. Cascaded multilevel symmetric inverters should have continuous DC sources. [16] –[21] consider inverters with equal DC sources, a reasonable assumption. Evolutionary algorithm finds Dc voltages and switching angles that reduce THD.

Problem formulation

A PV inverter which is an important element in the PV system, is used to convert DC power from the solar modules in to AC power which is to fed into the grid. Because of size, weight and price in favour of high frequency transformers, the aptitude is to remove the line frequency transformer when designing the new inverter. Furthermore, the existence of the high frequency transformer desires several power stages, as a result, reducing cost and increasing efficiency will be a challenging task. Thus, transformer-less grid-connected PV inverters offer cheaper cost, higher efficiency, smaller size, and weight.

Without the transformer, the electricity grid and PV module are galvanically connected. Therefore the fluctuating common mode voltage is generated between the PV module and the ground, as a result leakage current flows through the loop consisting of the parasitic capacitors, the filter inductors, the bridge and the utility grid.

This common mode leakage current increases the grid current harmonics and system losses and also creates a strong conducted and radiated electromagnetic interference. The existence of the leakage current increases grid current harmonics and system losses, deteriorates the electromagnetic compatibility and more significantly lead to a safety threat.

In order to counter these problems, the transformer less grid tied topology is proposed which minimizes the common mode leakage current and improves the efficiency of the system. Also the proposed grid tied transformer less topology can generate a multilevel waveform at the output voltage terminal which leads to a reduction in total harmonic distortion (THD) as well as decrease in electromagnetic interference.

Methodology

The structure of proposed grid tied inverter is indicated in Fig.14. As shown in this figure, the proposed topology consists of six power switches, two power diodes, two capacitors and an inductor. The power switches are of unidirectional type with antiparallel diodes. The overall operation of the

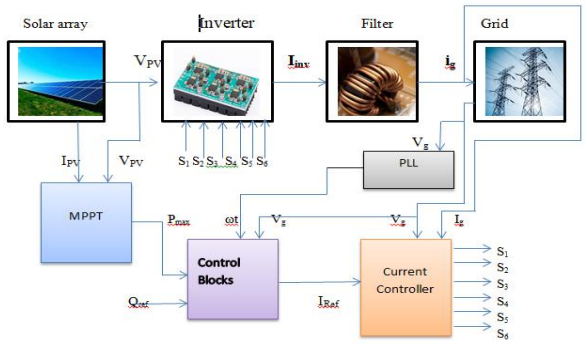

Fig 1: Block diagram of The Proposed System

Mathematical model of switched capacitor based MLI

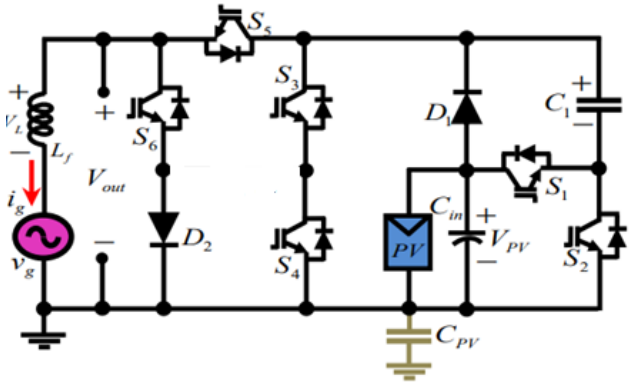

Fig 2: Proposed Single Phase MLI

system is based on series-parallel switching of the capacitors which makes the capacitors act as a virtual dc link similar to the techniques utilized in conventional multilevel inverters. By charging and discharging the capacitors, the proposed topology is able to boost the input source PV voltage with only a single stage. In addition, the negative terminal of the PV source is directly connected to the null of the grid which allows common ground capability with the proposed topology. Moreover, the inductor is acting as the output filter to smooth the output current waveform. Considering the same polarity of the grid voltage and the injected current to the grid, six different operating modes can be evaluated as depicted in Fig.3 (a)–(f). The switching states for the proposed Grid-Tied

inverter are addressed in Table I. In this table the charging and discharging mode of the capacitors are shown by 1 and 0, respectively.

The operating modes of Switched Capacitor based 5 level inverter are as follows:

Mode-1 : In the first operating mode, the switches S2 and S5 are ON. The grid voltage is positive and C1 is in parallel with the input voltage. Therefore, the voltage of C1 increases and the inductor current rises, Hence, the output voltage will be +VPV.

Mode-2: In the second operating mode, the grid voltage is still positive, but switches S1, S3, and S6 are turned on to reduce the inductor current to satisfy the volt-second balance principle and charge the capacitor C2. This generates a zero output voltage waveform. This setting reduces inductor current.

Mode-3 : Third-mode switches S1, S3, and S5 are activated. This mode charges capacitor C2 and outputs $+2V_{PV}$.

Mode-4: Negative grid voltage In the fourth operating mode, C1 capacitor voltages and switches S2, S3, and S6 inject power to the grid. Turning on switches S2, S3, and S6 turns off the power diode D2 and charges C1 to the PV voltage again. The inductor current linearly climbs in negative polarity as C1 discharges.

Mode-V: In the fifth operating mode, the inductor current reduces to negative polarity and charges the capacitor C1 to double PV Voltage. S1, S3, and S6 are activated.

Mode-VI: Finally, the last mode occurs when the switches S2, S4 and S6 are turned on. In this mode the capacitor C1 is discharged while C_{in} is charged by the input PV panel. Therefore, the $-2V_{PV}$ level is again created in the negative half-cycle of the grid's voltage.

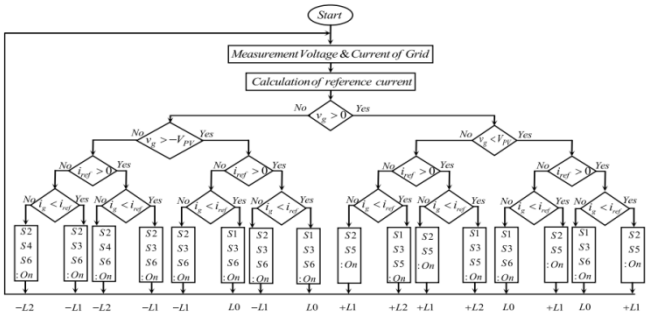

Fig 3: **PCC operation and Switching flow chart**

DESIGN PARAMETERS

A.Determination of L

Using inductor volt-second balanced principle across the output in the third operating mode for the sampling period,the switching duty cycle can be obtained

$$\int_0^{DTsw}(2V_{pv}-v_g)\ \mathrm{dt} + \int_{DT_{sw}}^{T_{sw}}(V_{pv}-v_g)\mathrm{dt} = 0 \qquad (1)$$

$$\mathrm{D} = \frac{v_g}{V_{pv}} - 1 \qquad (2)$$

The current equation of the inductor within a full period of the switching can be expressed as

$$i_L(\mathrm{t}) = \frac{1}{L}\int_0^t V_L(\mathrm{t})\ \mathrm{dt} + i_L(0) \qquad (3)$$

The current ripple of the inductor current will be

$$\Delta I_L = \frac{(2V_{PV} - v_g)D}{f_{sw}\, L} \quad (4)$$

Substituting the value of D from equ-2 we have

$$\Delta I_L = \frac{(3v_g - 2V_{pv} - {v_g}^2/V_{pv})}{f_{sw} L}$$

Where f_{sw} is the switching frequency.

The maximum value of current ripple occurs during the peak value of grid voltage

Therefore the final value of inductor L is obtained as

$$L = = \frac{(3v_g - 2V_{pv} - {v_g}^2/V_{pv})}{f_{sw}\Delta I_L}$$

By putting the experimental values as

$v_{gmax} = 230\,V$, $V_{pv} = 180V$, $f_{sw} = 50\,kHz$ and $\Delta I_L = 10\%\, of\, I_{gmax} = 0.3A$

$L = 2.6$ mH

B. Determination of capacitance

During the 4th and 6th mode of operation the discharge current of capacitor C1 is same as the inductor current.so voltage across the capacitor is

$$V_{C_2}(t) = \frac{1}{C_1}\int_0^t i_{C_2}(t)\,\mathrm{dt} + v_{C_1}(0) \quad (5)$$

So the voltage ripple of the capacitor is

$$\Delta V_{C_2} = \frac{i_L}{2f_{sw}\, C_2}\left(\frac{v_g}{V_{pv}} - 1\right) \quad (6)$$

The maximum value of ripple for C2 is achieved once the grid voltage and the inductor current reaches the peak. So, the value of C2 can be calculated as:

$$\boldsymbol{C_2} = \frac{I_{mg}}{2f_{sw}\,\Delta V_{C_{2max}}}\left(\frac{V_{mg}}{V_{pv}} - 1\right) \quad (7)$$

However, by taking the average value of the grid voltage and inductor current, the precise value of C2 is obtained according to (8), since the charging process of C2 is in the positive half-cycle of the grid voltage.

$$\boldsymbol{C_2} = \frac{2I_{mg}}{f_{sw}\,\pi^2\Delta V_{C_{2max}}}\left(\frac{V_{mg}}{V_{pv}} - \frac{\pi}{2}\right) \quad (8)$$

By putting the practical values in the above equations, we get

$C_2 = 680\mu F$ and $C_1 = 120\mu F$

Simulation

MATLAB Function 1

```
function taninv = fcn(q,p)

taninv = atan(q/p);
```

MATLAB Function 2

```
function sine = fcn(wt,q)

sine = sin(wt-q);
```

MATLAB Function 3

```
function y = fcn(p,q,v)

a = (p^2);

b = (q^2);

c = a+b;

d = 2*sqrt( c);

y = d/v;
```

MPPT Block Subsystem

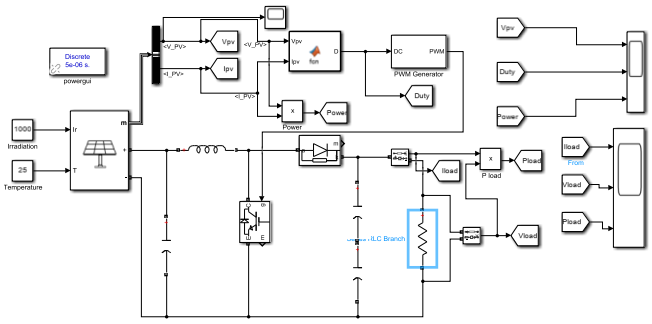

Fig 4: **MPPT Block Subsystem**

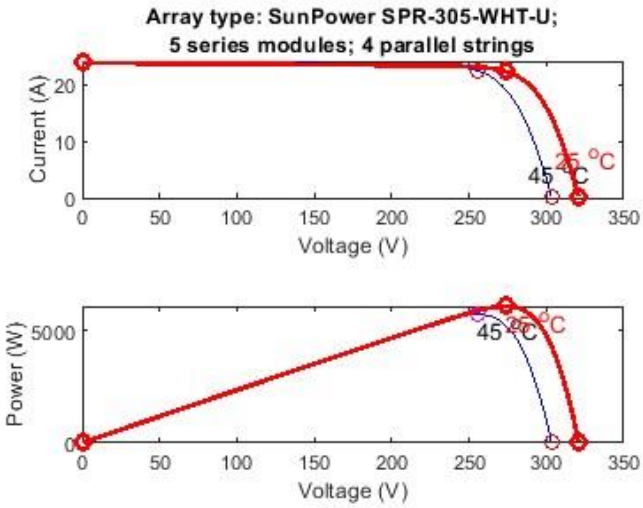

Fig 5: **VI and Power curv of the PV model**

P&O MATLAB Function

```
function D = fcn(Vpv,Ipv)
Dinit=0.4;
Dmax=0.9;
Dmin=0.1;
deltaD=25e-6;

persistent Vold Pold Dold;

dataType="double";

if isempty(Vold)
   Vold=0;
   Pold=0;
   Dold=Dinit;
end
P= Vpv*Ipv;
dV=Vpv-Vold;
dP=P-Pold;

if dP~=0
   if dP<0
      if dV<0
         D=Dold-deltaD;
      else
         D=Dold+deltaD;
      end
   else
      if dV>0
         D=Dold+deltaD;
      else
         D=Dold-deltaD;
      end
   end
else
   D=Dold;
end

Dold=D;
Vold=Vpv;
Pold=P;
```

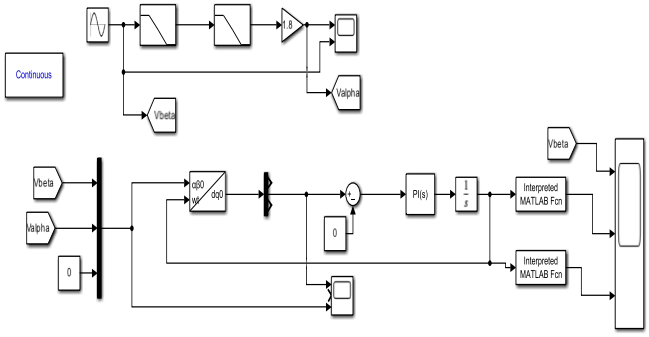

Fig 6: PLL Sub system

Results

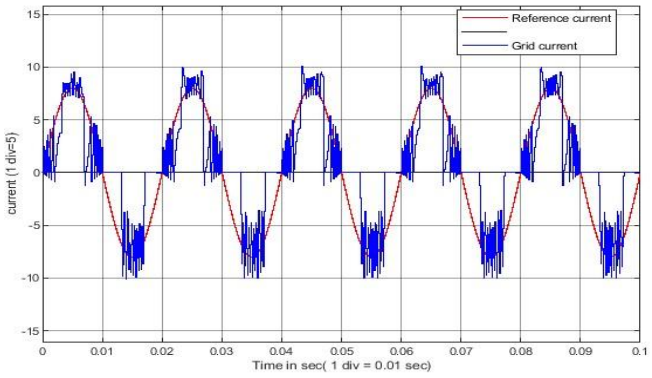

Fig 7: comparison between grid current and referrence current

In the above figure the grid current i_g is compared with the reference current i_{ref} . The grid current has a peak to peak value of 10 amp that of reference current is 8 amp.

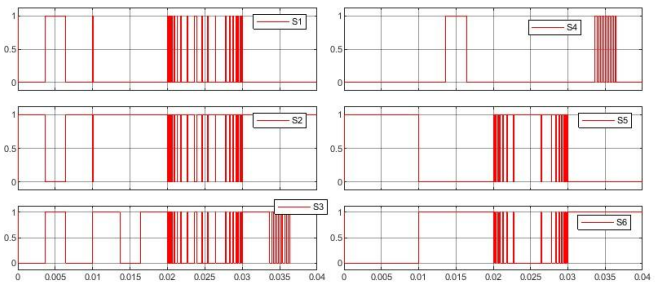

Fig 8 **: switching pulses of IGBTs**

In the above figure, the gating pulses of the six power switches (IGBTs) are shown. 1 indicates that switch is ON and 0 indicates the switch is OFF.

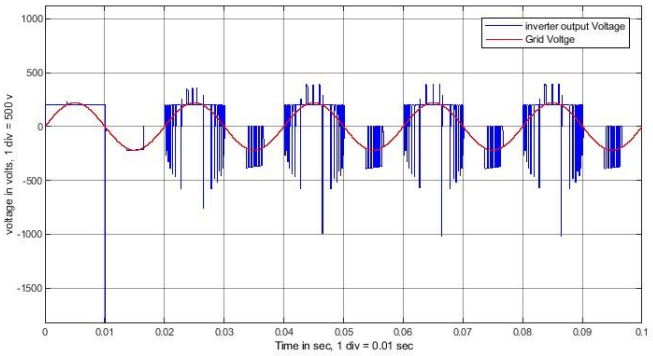

Fig 9: **inverter output voltage and grid voltage**

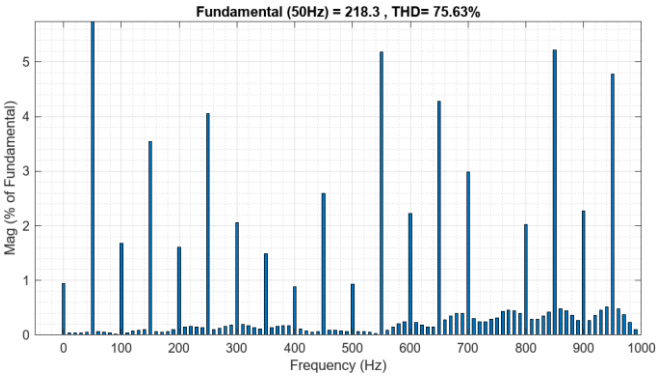

Fig 10: **THD of inverter output voltage**

Conclusion

This article analyzes the output voltage and harmonic spectrum of a PCC-based, switched-capacitor multilayer grid-tied inverter. The series-parallel switching method of capacitors is aided by the proposed topology, which also provides the benefits of a common ground. In addition, the suggested inverter's output voltage terminal multilayer waveform generates low total harmonic distortion. Series parallel switching conversion keeps the capacitors in

the SC module of the proposed inverter in good balance so that they can manage the single stage power boosting operation for both the positive and negative half cycles of the grid frequency. Regarding the examined PCC method, any desired PF can be achieved by injecting a current through a filter based on a tiny inductor size into the grid. The issue of leakage current is also fully removed because the null of the grid and the negative terminal of the input source (PV panel) share a common ground. However, the output voltage's THD is displaying as 75.63% at a fundamental value of 218.3V due to a simulation error.

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