DESIGN A COMPACT MODEL OF SPIN TRANSFER TORQUE MRAM WITH MAGNETIC TUNNEL JUNCTION

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Abstract: *This study describes the design, construction, and modeling of a magnetic tunnel junction-based Spin Transfer Torque Random Access Memory (STT-MRAM). Spin Transfer Torque Magnetic Random Access Memory (STT-MTJ-MRAM) was used in the tests. Various findings are demonstrated about the relationship between voltage and magnetization components in different directions, as well as the dependence on damping factor and precision. Additionally, the paper presents voltage-current graphs that depict the dependence on torque and variation of output voltage concerning time. The results provide valuable insights into the behavior and performance of STT-MTJ-MRAM in various operating scenarios. Furthermore, the paper discusses the variations in bit line voltage, digital output voltage, pre-charge voltage, word transfer operation, read operation, and write operation. Additionally, the paper presents the changes in phase angle and azimuth angle with respect to time and the magnetization's strength in different directions over time.*

Keyword: *Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM), Magnetic Tunnel Junction (MTJ), Spin Transfer Torque MRAM with Magnetic Tunnel Junction (STT-MTJ-MRAM), Voltage and magnetization relationship, Damping factor*

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INTRODUCTION

Conventional Complementary Metal Oxide Semiconductor (CMOS)-based Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) are limited by power consumption limits due to the decreasing size of the semiconductor production process. It is possible to tackle this problem by building non-volatile main and cache memory. This system may run in sleep mode without losing data and eliminates static power consumption and leakage current [1]. In addition to charge storage and data transmission, spintronics, a new branch of science and engineering, uses electronic spin. To improve the overall functioning of spintronics, spin transistors, for instance, are being researched in this field [2].

Small models, usually based on analytical equations, are heavily used in the design of circuits [3]. Studies in which miniature versions of Spin Transfer Torque-Magnetic Tunnel Junctions (STT-MTJs) are used have recently attracted a lot of interest. In some compact models [4], MTJ dynamic equations are easily solved. The following are just a few of the many advantages of using STT-MRAM: [5],

- Non-volatility
- High endurance
- High-speed operation
- Low power dissipation

1.1 Magnetic Tunnel Junction

Simulating and designing MTJ-based STT-MRAM requires an accurate and effective model. The model must be compatible with SPICE and other circuit simulators, accurately represent the MTJ, and provide a thorough physical description. This includes making use of behavioral and micromodels (micromagnetic) for improved depiction [6].

The Giant Magneto Resistance (GMR) effect opened the door for the creation of spintronics devices [7]. The Magnetoresistive Tunnel Junction stands out among these gadgets as a potential replacement for traditional memory like SRAM. Sandwiching a nonmagnetic layer between two ferromagnetic layers produces the tunnel magnetoresistance (TMR) phenomenon, as seen in Figure 1.

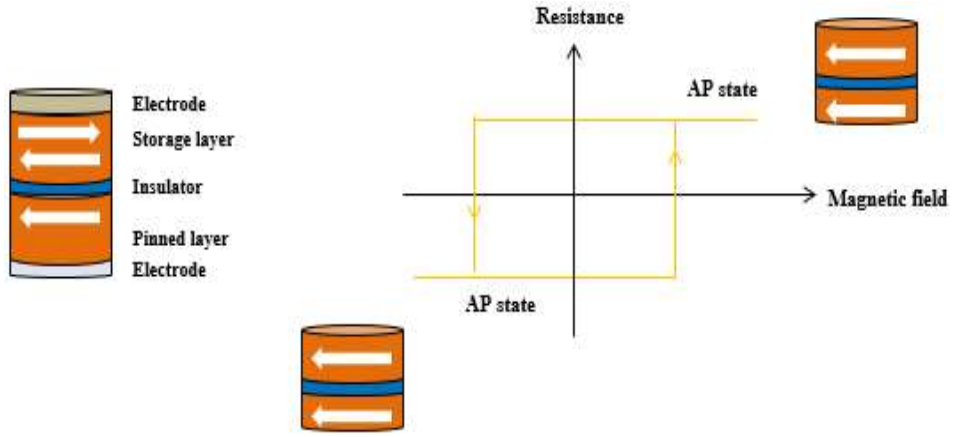

Figure 1: Structure of Magnetic Tunnel Junction [8].

The discovery of the GMR effect led to the development of spintronic devices. The MTJ has the potential to take the place of current memories like SRAM because it is a crucial spintronics technology. MTJ is constructed of three layers: two ferromagnetic and one nonmagnetic. In this construction, Julliere discovered the Tunnel Magneto Resistance (TMR) effect [8]. The equation shown below could be used to express these features mathematically:

$$TMR = \frac{R_{AP}-R_P}{R_P} \qquad (1)$$

The magnetic tunnel junction (MTJ) is a metal–insulator–metal structure with two CoFeB ferromagnetic electrodes separated by a thin MgO tunnel barrier (tMgO ≈1 nm). Each of these electrodes is referred to as the pinned layer (PL) because of its fixed magnetic polarisation, while the free layer (FL) could vary its polarization from parallel (P) to antiparallel (AP) concerning the PL. The tunnel magnetoresistance (TMR) effect causes the MTJ resistance to change depending on the direction of the magnetic polarisation of the FL and PL [9]. A spin-transfer torque (STT) causes the FL magnetic polarisation to change when electrons flow over the MTJ, accomplished by the conservation of angular momentum [10].

1.2 MTJ-based STT-MRAM System

Spin-transfer-torque magnetic random-access memory (STT-MRAM) has attracted a lot of attention as a potential candidate for the forthcoming generation of high-density integrated non-volatile memory. [11]. A magnetic tunnel junction stores the information in the memory [12]. In general, it is far more trustworthy than magnetic quantum cellular automata. As shown in Figure 2, MTJ is a bit-memory cell that might store information in artificial neurons and synapses, nanomagnets, Bayesian inference engines, Boolean logic gates, and Boltzmann machines. Three elliptical layers make up this construction [13]. Between an insulator and a spacer layer are ferromagnetic outer layers. One of the ferromagnetic layers in one of the two stable orientations is a hard or fixed ferromagnetic layer with permanently aligned magnetization. Another choice is to utilize a soft or free layer of ferromagnetic material, which can have its magnetism point in one of two stable directions and encodes the bit information. The electrical resistance between the two ferromagnetic layers could be used to decode the encoding bit of the soft layer. The resistance drops dramatically when the two layers' magnetizations are parallel, but jumps up dramatically when they're antiparallel. [14].

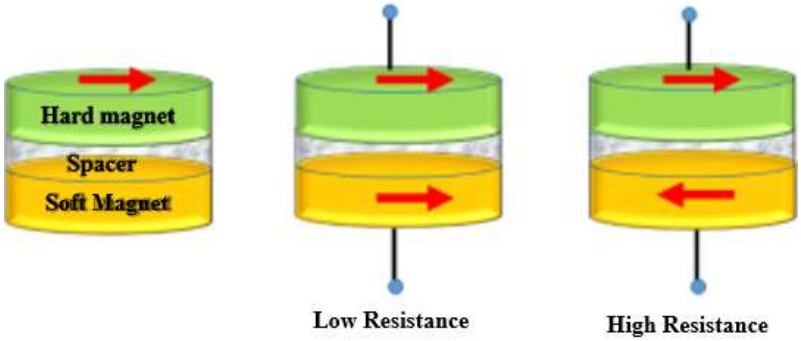

Figure 2: Low Resistance & High Resistance [15].

STT-MRAM (a kind of magneto-resistive random-access memory), which uses spinning-to-rotating torque as an example of a spintronic circuit, has advanced significantly in recent years [16]. Since flash memory (conventional non-volatile memory) has a low write endurance (10^5) and a high write access time compared to other non-volatile memory technologies (10^5 to 10^7 sec), while ferroelectric (FeRAM) and phase-change memory (PRAM) have written endurances of 10^9 to 10^{12}, respectively, STT-MRAM is a strong contender for universal memory. STT-MRAM, on the other hand, has a quick access time (in the range of nanoseconds) and high endurance (about 10^{15}) [17].

2. REVIEW OF LITERATURE

Table 1 summarizes the results of the literature review, which are described below. This part describes reviews of past work pertaining to Spin Transfer Torque MRAM involving Magnetic Tunnel Junction.

Table 1: Analytical Comparison of the Existing Literature.

Authors	Technique Used	Outcome	Research Gap
Garzón et al., [18]	A DMTJ device.	It is possible to obtain higher energy efficiency when performing combined write and read operations.	The authors want to further investigate this paradigm in the future to reduce read latency.
Wang et al., [19]	A new CiM platform that saves space.	The 40 nm technology node hybrid spintronic/CMOS simulations validate the proposed CiM platform's functionality and performance.	The design concept would allow the authors to perform sophisticated operations like full-adder (FA) and XOR/XNOR with the help of RLM's fast speed and WLM's integrity.
Wang et al., [20]	Perpendicular Magnetic Anisotropy (PMA) double barrier Ta/CoFeB/MgO compact physics model.	Magnetic full-adder (MFA) has been built and tested as an example of a hybrid logic-in-memory circuit.	The PMA-MTJ structure of CoFeB/MgO/CoFeB will be studied further using a spice-compact model incorporating STT stochastic behavior.

Prajapati et al., [21]	PMA and In-plane magnetic anisotropy (IMA) are two types of magnetic anisotropy	A good agreement was found between the sMLC and pMLC STT-MRAM designs with an average variance of less than 5%.	MRAM designers would focus on two-bit series (sMLC) and parallel-MLC designs utilizing voltage-controlled spin.
Wang et al., [22]	Spintronic memory (NAND-SPIN) based on the NAND architecture.	Writing NAND-SPIN at 28 nm nodes could reduce write energy by 3 – 5 times and bit-cell area by 2 – 4 times over SOT-MRAM.	For ultrafast computing, the scientists intend to conduct more research on toggling spin torque magnetic random-access memory.
Deng et al., [23]	NV-FA is an 8-bit synchronous non-volatile full-adder design.	To construct a truly usually-off system that meets the needs of many applications, more complicated logic circuits might be designed.	In the future, researchers will develop a non-volatile magnetic full-adder (MFA) circuit that could power the gate without losing data.
Vincent et al., [4]	The stochastic switching delay is represented as an analytical model.	MRAM designs that use an analytical model could have lower error rates than those that do not.	Spin-transfer torque magnetic random-access memories multi-level cell (MLC) structure, which includes two transistors and two magnetic tunnel junctions (MTJs), will be examined in future studies (STT-RAM).
Lim et al., [5]	Model at the level of the circuit.	More accurate circuit-level modeling is achieved by including the temperature and voltage features of MTJs.	Future studies could use the switching behavior model to provide a technique for dynamic current monitoring.
Cai et al., [24]	CSME	The simulation's slight improvement of 2.4 and 14.1 percent in read error rates benefits low Vdd (0.6 V) and low TMR (50 percent) sensing conditions.	More study is required to test the suggested design's performance and yield on larger-scale platforms and to determine whether or not it can be integrated with more sophisticated CMOS technology nodes.
Wang et al., [25]	Spin transfer torque (STT) switching method	This study examines MTJ's behavior at different temperatures and provides a model to	This research could involve investigating novel materials, device structures, or circuit

		maximize STT-MRAM's dynamic operations and temperature tolerance.	architectures that can mitigate the negative impact of temperature on MTJ performance.

3. Problem Formulation and Research Gap

A promising non-volatile memory technology known as magnetic tunnel junctions is anticipated to be used in the next generation of universal memory. STT-MRAM excels in longevity, retention, access speed, and power consumption among the numerous alternatives, making it a standout performance. Specific sensing approaches, such as toggling spin torque and leveraging magnetic RAM for quick computation, were taken into consideration to enhance an STT-MRAM's Magnetic Tunnel Junction. The promise of this technology was shown by how these approaches boosted the typical reading speed while lowering the specific power consumption.

Following research gaps must be filled to improve the design and functionality of MTJs and STT-MRAM technology:

- STT-RAM durability and reliability issues are brought on by read current disturbance and aging of the ultrathin tunnel barrier when the cell area is reduced to satisfy density and power specifications.
- Variations in data and reference cell resistance are less of an issue with a Sense Amplifier.
- Thermal changes substantially influence STT-MRAM devices, which restricts their ability to scale. STT-MRAM devices have previously suffered from issues, including MTJ manufacturing differences and the CMOS access transistor.

4. METHODOLOGY

The proposed technique, which intends to examine the effect of toggling spin torque magnetic RAM on boosting average reading speed and cutting average power consumption, is fully described in this part. The improvement of the sensing margin is the primary goal of this research. The approach uses the magnetic switching spin transfer switching model to accomplish this goal. The local bit line's installation also results in a decrease in average power. The process is thoroughly explained in the part that follows:

4.1 Endurance and Reliability Issues in STT-MRAM

Several important reliability problems are addressed during read and write operations on STT-MRAM [26]. Coupling faults, write polarization asymmetries, and transition faults are the three basic categories of write reliability problems. Poor read reliability includes memory issues, inaccurate readings, read interruptions, and judgment errors.

Several physical variables affect the read reliability of MRAM [27]. One of the most significant macroscopic factors affecting the sensing margin is the limited TMR. Due to the overlap in the distribution of RAP/RP in the tails, restricted TMR yields identical parallel resistance (RP) and anti-parallel resistance (RAP) ratios. Even though the MRAM sensing block uses an ideal reference cell [28], SA is unable to differentiate between the low state and the state of MTJ. Several elements influence the reliability of STT-MRAM, some of which are included in Tables 2 and 3.

Table 2: Causes and mechanisms of poor writing and reading.

Affect	Mechanism	Key Cause
Read	Read disturb	Growing with technology scaling Read and write and assign the same path
	Incorrect read fault	Short sensing boundary window of VSA Opposite temp. reliance resistance Parasitic impacts

	Retention failures	Thermal noise Intrinsic thermal instability
	Decision Fault	Low supply voltage Process variations Limited TMR
Write	Coupling faults	Neighboring cells changing
	Write polarity irregularity	P to AP needs higher shifting current
	Transition faults	Thermal fluctuations Stochastic nature of writing operation

Table 3: STT-MRAM Reliability Influencing Factors.

MTJ parameters	**Transistor parameters**
The saturation magnetization (MS)	transistor (VT)
Magnetic anisotropy (HK)	The threshold voltage for a user's access.
Tunnel magneto-resistance ratio (TMR)	Access route length and width alterations in the transistor.
Oxide thickness of MgO level (tox)	
Planar lengths of the MTJ	

4.2 Magnetic Switching

MTJ's switching strategies are consistently under investigation as potential memory contenders [31]. Initial implementations of Magneto-resistive Random-Access Memory (MRRAM) utilized field-induced magnetic switching (FIMS). However, FIMS faces challenges in achieving energy efficiency and low power consumption due to its high-power consumption, large die area, and significant disruptions.

In 2003, Thermally Assisted Switching (TAS) for MTJ was introduced to reduce the switching current threshold. This technique involves heating the MTJ to enhance its switchability by passing a current across it [32]. However, the scaling problem persists even after cooling down following the heating process. Consequently, the switching speed must be reduced to maintain TAS's low power consumption (less than 1 mA).

A newer switching approach, Spin Transfer Torque (STT), addresses power and scalability issues. It enables high-density and low-power MRAM without relying on magnetic fields, as the MTJ is switched on and off using a lower current (100 uA) [33]. Shoji Ikeda et al. achieved high thermal stability using interfacial PMA MTJ.

To overcome the incubation delay caused by STT switching, researchers have explored the spin hall effect as an assisted switching method. The combination of the spin hall effect and STT (SHE plus STT) mitigates the incubation delay, which is a drawback of the regular STT method. By using a three-terminal arrangement, this technique allows for the complete separation of the writing and sensing functions [34]. It achieves low resistance for writing and high resistance for detecting, making almost a tenfold reduction in switching current possible.

4.3 Spin Transfer Torque Switching Model

MTJ switching behavior was modeled using Slonczewski's [35] Spin-Transfer Torque physics model in the micromod. One of the most significant contributions of this model is the explanation of how the critical current could be obtained.

$$J_{C0} = \alpha \times \gamma \times \gamma \times e \times M_S \times t \times (H_{ext} \pm H_{ani} \pm \frac{H_d}{2})/\mu_B \times g \quad (2)$$

$$E = \frac{M_s \times V \times H_C}{2} \quad (3)$$

$$g = [-4 + (P^{-1/2} + P^{1/2}) \times (3 + cos\,\theta)/4]^{-1} \quad (4)$$

$$J_C = J_{C0}\{1 - (\frac{K_B \times T}{E}) ln(\tau \times f_0)\} \quad (5)$$

$$I_C = J_C \times surface \quad (6)$$

- **Constants:**

H_{ext}: The external field: -19Oe
H_{ani}: 100 Oe of in-plane uniaxial magnetic anisotropy.
H_d: Demagnetization field 13000 Oe induces an out-of-plane magnetic anisotropy.
f_o: Attempts to use 109 Hz as a frequency.
K_B: Constant of Boltzmann, 1.38 $\times 10^{-23}$ J/K
u_B: The magneton constant of Bohr is 9.27 $\times$ 10^{-28} J/Oe.
M_s: 1.3 T (CoFe) =13000 Oe
H_c: Coercive field
α: Gilbert's coefficient of damping is 0.001.
γ: 221000/2*pi, a gyromagnetic constant
e: Elementary charge of 1.60 $\times$ 10^{-19} C.

- **Parameters:**

t: The free layer's height (1-3nm).
V: (80×240 nm^2 ×t) is the volume of the free layer

5. Implementation Results using LTspice and MATLAB tools.

In this part, we present a more basic version of Spin Transfer Torque MRAM (STT-MRAM) which relies on a connection made possible by a magnetic tunnel junction. The stated model is meant to be understandable by the average reader, giving them access to the benefits of STT-MRAM. The following are the findings of experiments performed on STT MRAM. The MTJ input parameters are shown in Table 4.

Table 4: Input Parameters for MTJ Subcircuit

lx	32n
ly	96n
lz	2.44n
Ms0	1210
P0	0.69
α	0.0062
Tmp0	358
RA0	5
MA	0
ini	1

The findings are shown in figure 3, which is available below. These results demonstrate waves in the voltage across magnetic tunnel junctions caused by noise during read and write operations. V (1) and V (2) indicate the voltage across magnetic tunnel junctions.

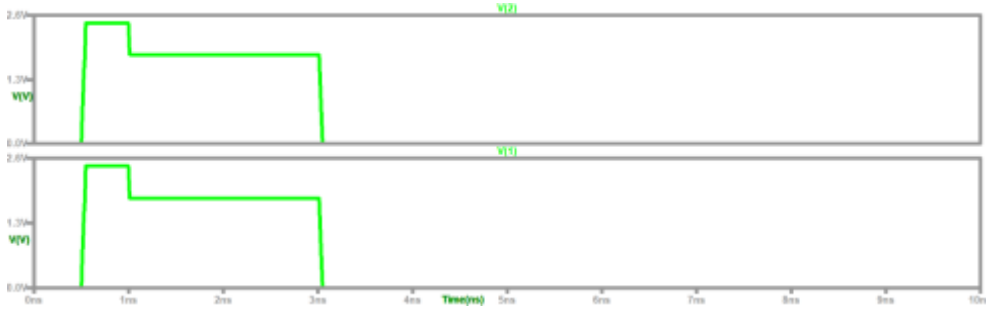

Figure 3: V (1) and V (2) show magnetic tunnel junction voltage.

The voltage against the x-axis segment of the free layer magnetization vector m is shown in figure 4. V(my) plots voltage against the y-axis segment of the free layer's magnetization vector m. The voltage V plotted against the z-component of the free layer magnetization vector m is denoted by the notation V(mz).

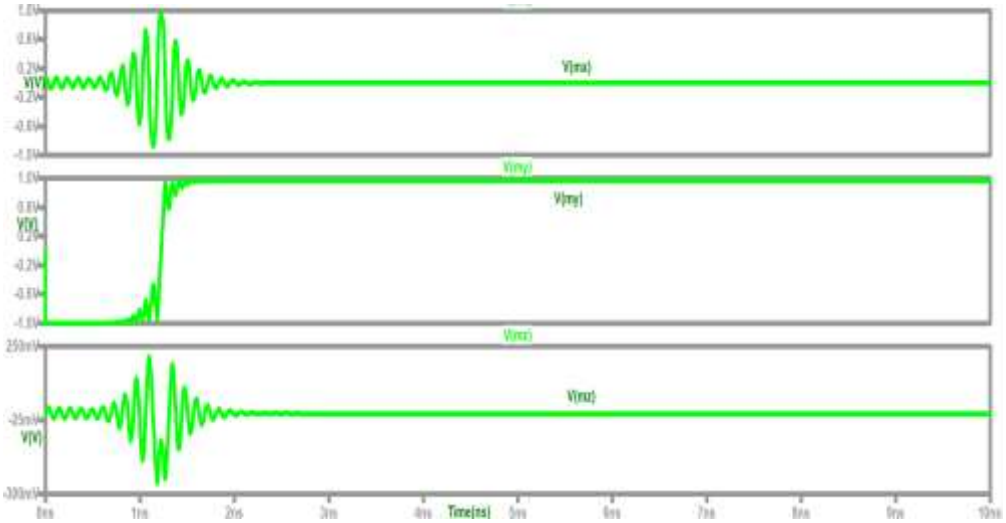

Figure 4: Voltage Vs Magnetization

Figure 5 depicts a graph that demonstrates a dependence on the damping factor in the x direction via a voltage-current plot. The x-axis represents the voltage (V) in the x-direction, while the y-axis represents the current (I) across the system. It shows the variation of voltage due to damping factor along the x, y and z directions with respect to time (ηsec).

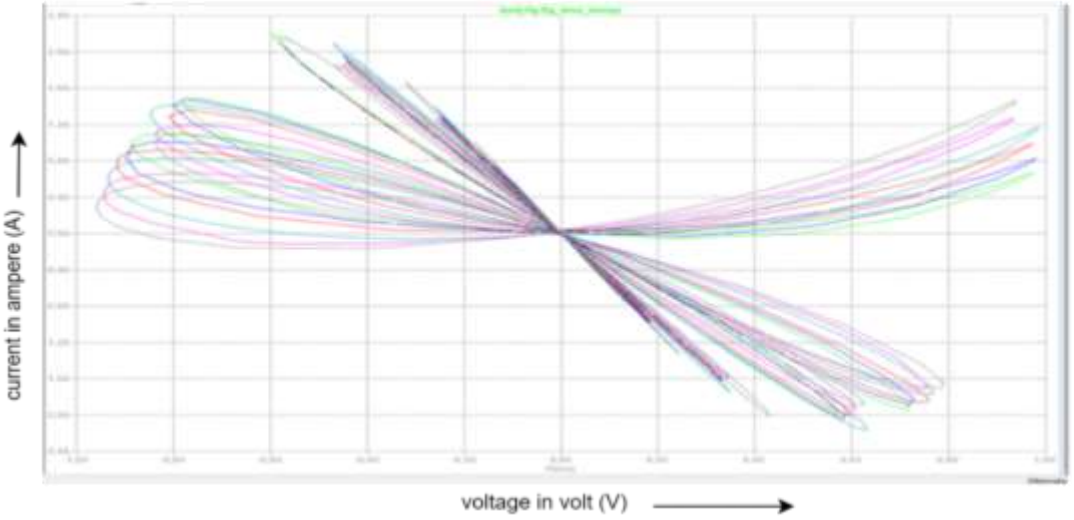

Figure 5: Voltage-current graph of damping factor along the x direction

The plot of voltage vs current along the y-axis is shown in figure 6, which represents the reliance on the damping factor.

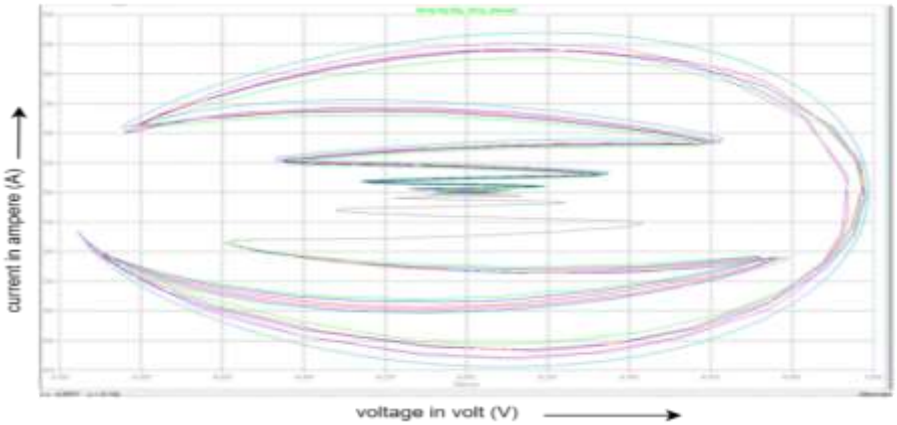

Figure 6: Voltage-current graph of damping factor along the y direction

The voltage-current plot that demonstrates the dependence on the damping factor is shown in figure 7 along the z-axis.

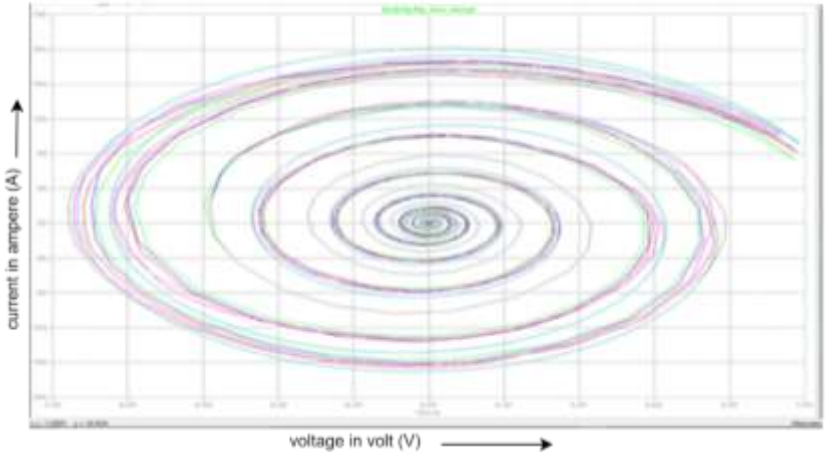

Figure 7: Voltage-current graph of damping factor along the z-direction

Figure 8 is a depiction of the voltage-current plot that demonstrates the dependence on precision along the x-axis.

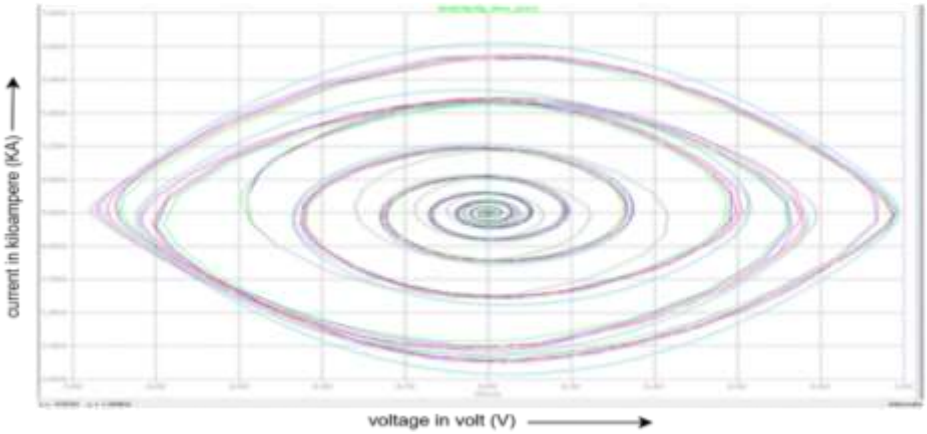

Figure 8: Precision-voltage-current plot along the x-axis

Figure 9 illustrates the trade-off between voltage and current, illustrating the dependence on precision along the y-axis.

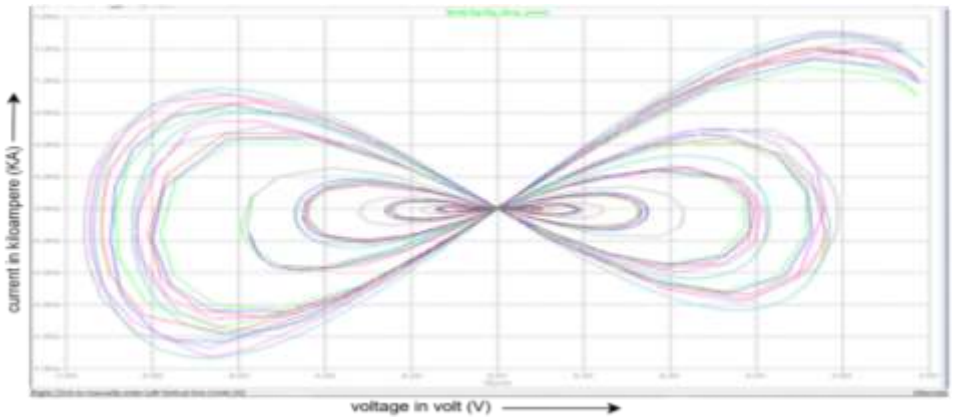

Figure 9: Precision-voltage-current plot along the y-axis

Figure 10 is a depiction of the voltage-current plot that demonstrates the dependence on precision along the z-axis.

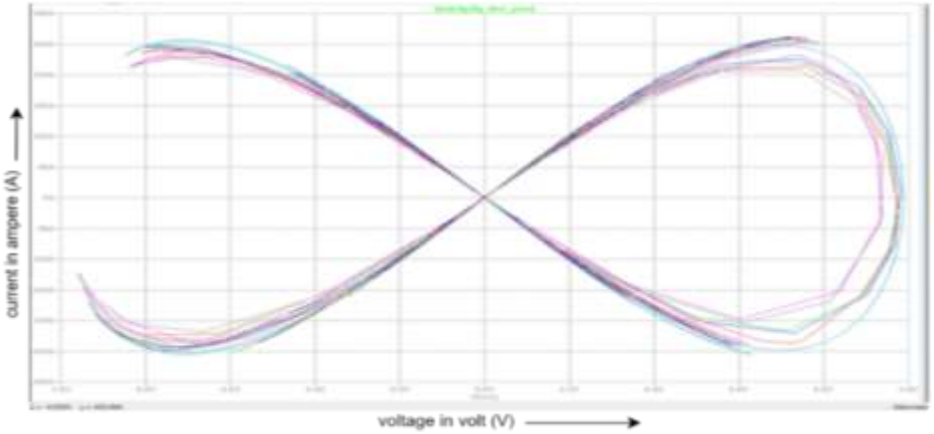

Figure 10: Precision-voltage-current plot along the z-axis.

Figure 11 is a depiction of the voltage-current graph that demonstrates the dependence on torque in the x direction.

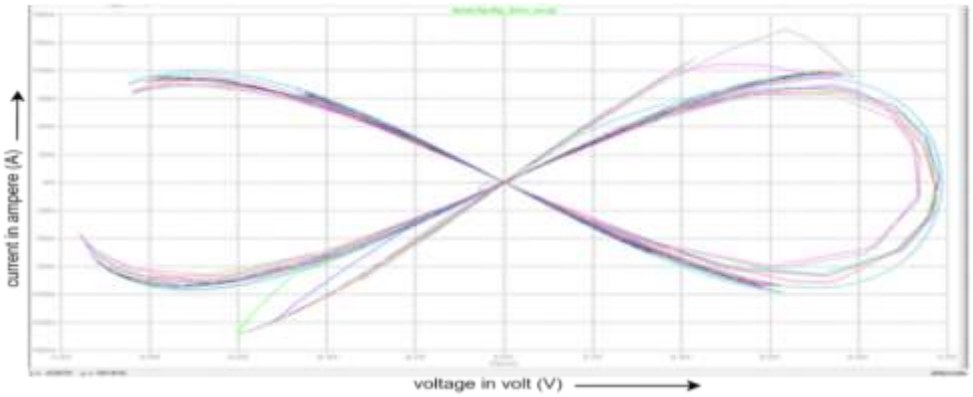

Figure 11: Voltage-current graph of torque-x direction dependence

Figure 12 is a depiction of the voltage-current plot that demonstrates the dependence on torque in the y direction.

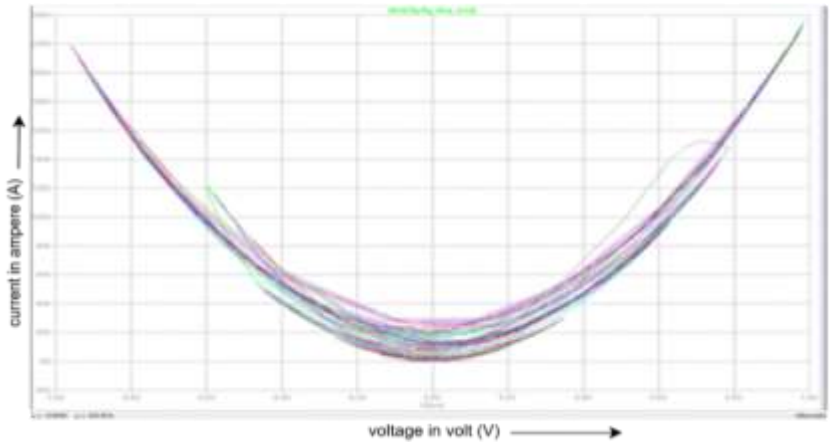

Figure 12: voltage-current graph of torque on y-direction dependence

Figure 13 is a plot of voltage against the current that illustrates the dependence of torque in the z-direction.

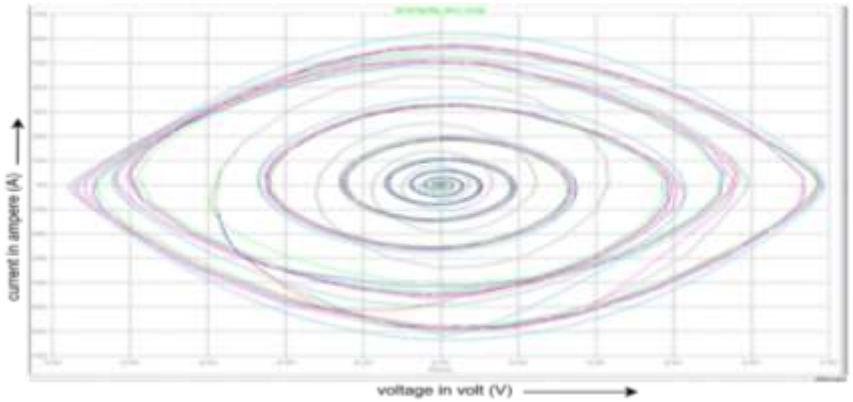

Figure 13: voltage-current graph of torque-z direction dependence

Stt-Mtj-Mram

Figure 14 shows how magnetic tunnel junctions (MTJs) can be used in embedded memory applications like Spin Transfer Torque Magneto-Resistive Random-Access Memory (STT MRAM).

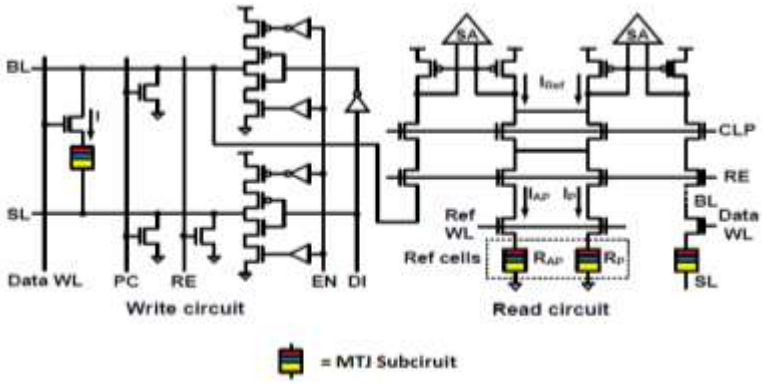

Figure 14: STT-MTJ-MRAM Circuit diagram for simulation

Table 5 illustrates the denotations of various situations of the time-voltage trade-off.

Table 5: The time-voltage trade-off for numerous situations

Variable	Meaning Of Variable
V_bit	Bit line voltage
V_d	Digital output voltage
Vd_bar	A time-dependent bit-line voltage difference of several cells throughout the read process.
V_pc	The precharge voltage supplied repeatedly
Vq_bar	A single side-NMOS sensing system measures the bit-line voltage difference of multiple cells throughout a read process relative to time.
V_read	Variation of voltage during the read operation
V_word	Variation of voltage during word transfer operation
V_write	Variation of voltage during the write operation
V_se	Parallel and anti-parallel resistance-voltage variation.

Operating waveforms of STT-MTJ-MRAM

The trade-off between the change of voltage regarding time for several possible scenarios of the operating waveforms of the proposed STT-MRAM is shown in Figure 15.

Figure 14: STT-MTJ-MRAM different waveforms during operation

The V_bit is a graphical depiction of the bit line voltage in terms of time in nanoseconds (ηsec). The V_d is a graphical representation that shows how the digital output voltage changes over time. The bit-line voltage disparity of different cells throughout the read operation is graphically represented over time by the Vd_bar, additionally referred to as Vd_out. This is accomplished through the utilization of a dual side-NMOS sensing scheme, which is successful despite the presence of Dual-transistor circuitry.

V_pc is a graphic representation of the relationship between the pre-charge voltage that is repeatedly given and its aspect to time. Vq_bar is a graphical representation of the bit-line variation in voltage of different cells recorded during the course of a read operation utilizing a single side-NMOS sensor device and time. This method is successful despite the presence of dual transistors and works effectively. The graphical depiction of the relationship between the fluctuation in voltage that occurs throughout the read operation concerning time is shown by the V_read variable.

The variable V_word displays a graphical depiction of the relationship between the changing voltage that occurs throughout the word transfer operation w.r.t time. The V_write creates a graphical depiction of the relationship between the changing voltage that occurs during the write operation and the passage of time. The V_se provides a graphical depiction of the relationship between the fluctuation in voltage concerning the resistance in both the anti-parallel and parallel modes. A higher voltage is observed for antiparallel signal orientations, whereas a lower value is observed for parallel signal orientations. Figure 16 represents the Change in phase angle (ϕ) concerning time (in ηsec).

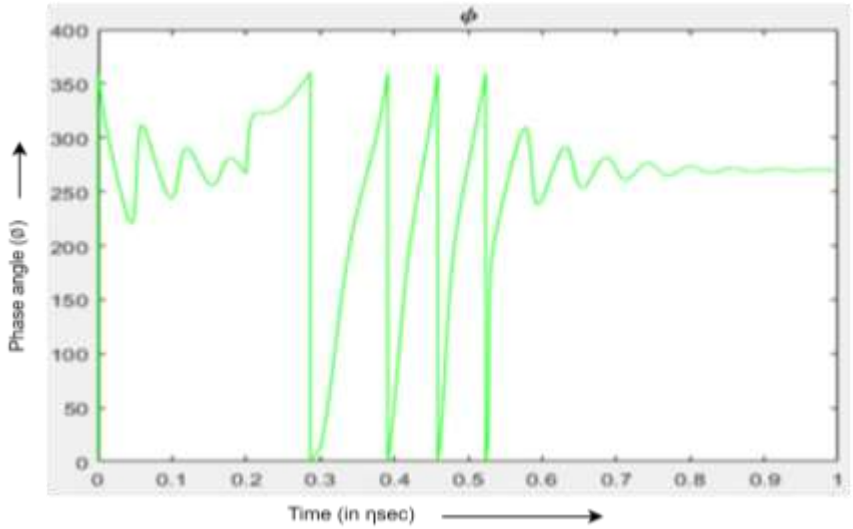

Figure 16: Phase angle ϕ vs. time (in ηsec).

Figure 17 depicts the change in azimuth angle (θ) with respect to time (in ηsec).

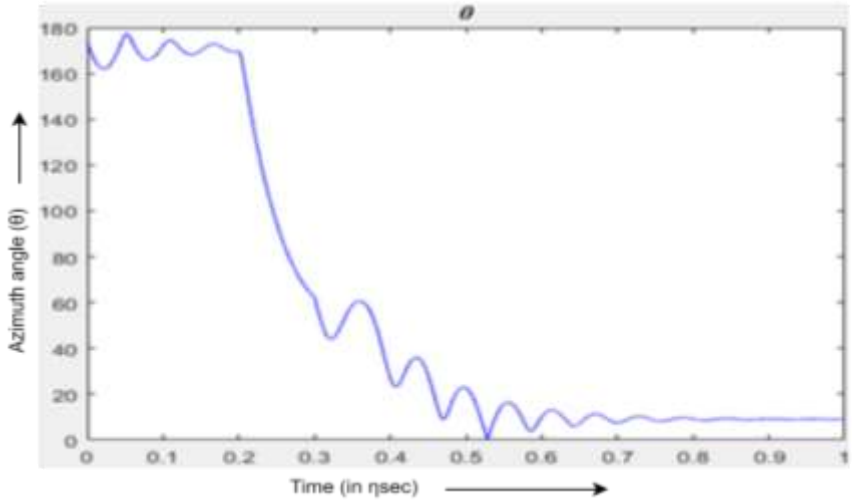

Figure 17: Azimuth angle (θ) vs. time (in ηsec).

Magnetization's varying strength in the x direction is shown over time (in ηsec) as shown in Figure 18.

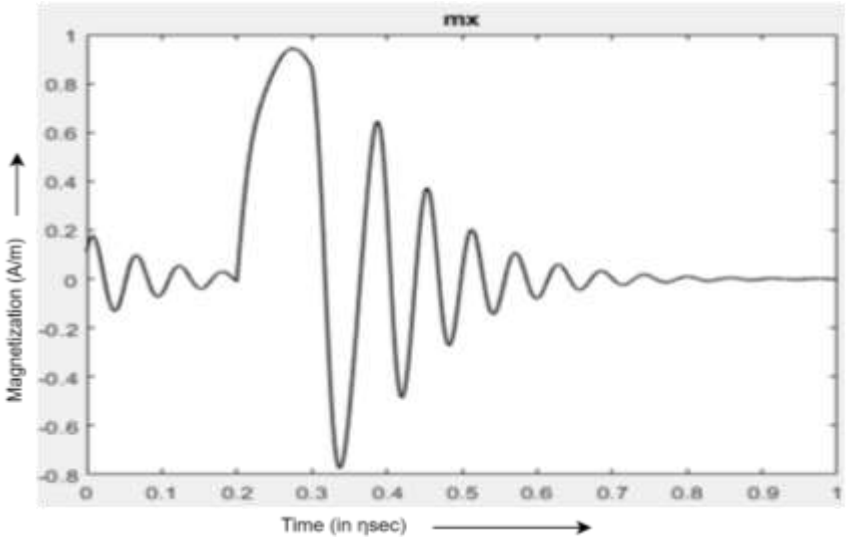

Figure 18: Magnetization along x direction vs. time (in ηsec).

Figure 19 presents the variation of magnetization along z axis w.r.t time (in ηsec).

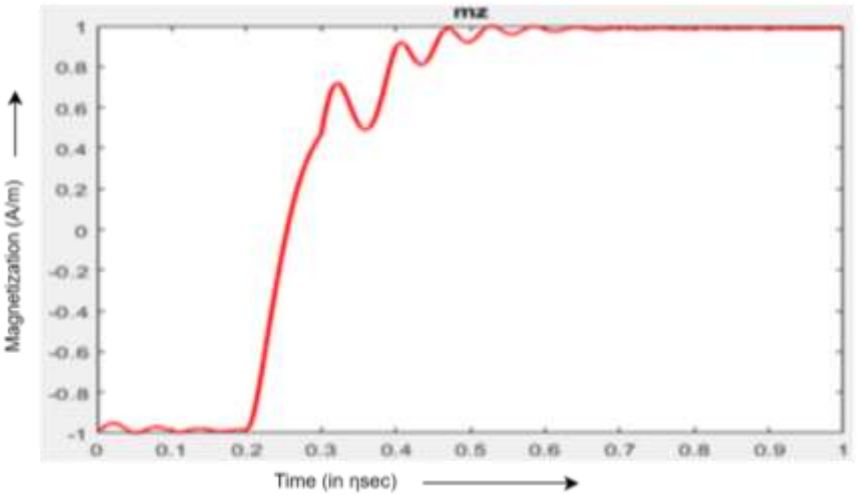

Figure 19: Magnetization along z axis w.r.t. time (in ηsec).

The magnetic field's three-dimensional fluctuation in the axes of x, y, and z is seen in Figure 20.

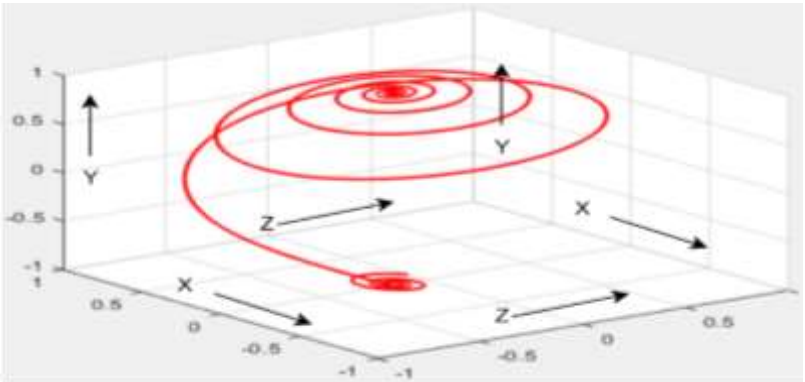

Figure 20: Three-dimensional magnetization field along the axes of the x, y, and z

Figure 21 shows the time-dependent power fluctuation (in ηsec).

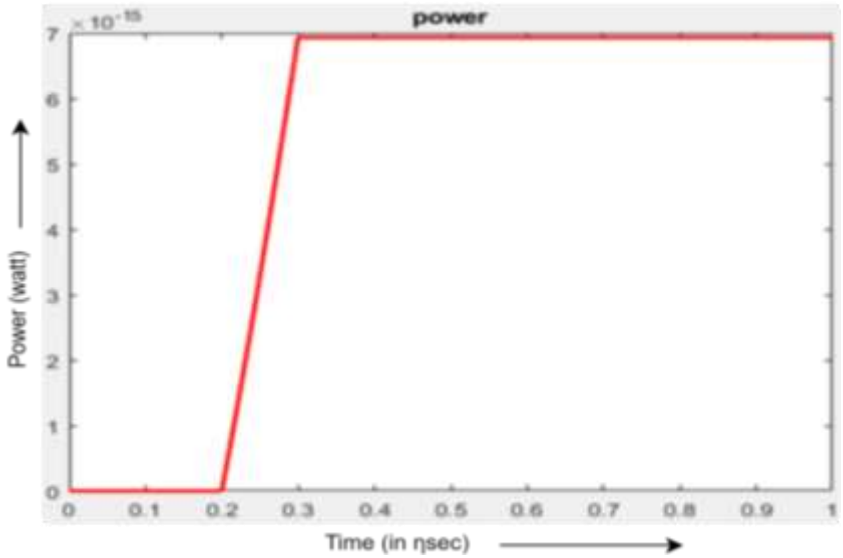

Figure 21: Power (in watt) w.r.t time (in ηsec).

6. CONCLUSION AND FUTURE SCOPE

Magneto-Random-Access Memory (MRAM) is a promising candidate for the future generation of memory due to its high level of density, flexibility, non-volatility, and quick operation. The STT MTJ (spin transfer torque magnetic tunnel junction) has shown great promise in the fields of magnetic logic and memory due to its fast throughput, low power consumption, and almost limitless lifespan. An abstract model of a multi-level static memory with random access that uses a spin transfer torque, and a tunnel junction of magnets is presented in this study. In this study, the author outlines the input values for the MTJ subcircuit and gives experimental findings to back up the claims stated in the study. Noise-induced voltage waves were discovered using LTspice and MATLAB models of magnetic tunnel junction during read/write operations, providing insight into the durability and performance of STT-MRAM devices. How the damping component, torque influenced the device's electrical characteristics was shown using voltage-current graphs. Positive results and promising future directions for Spin Transfer Torque MRAM using a MTJ have been provided in this research. The described results suggest that STT-MRAM technology has potential as a storage solution for future computer systems, and they will surely motivate more investigation and development in this field.

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