High Performance Multiplier Using Reversible Logic For Single Precision Floating point Numbers

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Abstract –The decisive performance factors for any electronic device are power dissipation and operating speed. The efficiency of any circuit depends on the performance of the processor built into it. Multipliers play an important role in any processor or computer system. This article describes four different 32-bit multiplier designs and compares the multiplier designs with high performance factors. In recent years, multiplier research has continued to reduce the quantity of some products in terms of delay and area. Which are the main factors limiting circuit performance in VLSI designs, to eliminate this problem, we introduce array multipliers and Vedic multipliers, which use logic reversible gates in full and half adders. With this design, the combined path delay, power and area are reduced. In reverse logic, one-to-one mapping between input and output is important strategy for reducing Power consumption. Many simple logic gates such as Fredkin, Feynman, Toffoli and Peres have been proposed and digital circuits are designed using these gates. A floating-point unit (FPU) is part of a computer that is specifically designed to work with floating-point numbers. Here, the floating points unit (FPU) follows the IEEE 754 precision format. This article simulates and demonstrates the design of a 32-bit single precision floating point multiplier is designed with reversible logic gates for better performance, Floating point number can support a wide range of values. It is represented using three fields: sign, exponent, mantissa. For performance metrics of this design, various parameters such as area, power and delay requirement are obtained and presented. We developed all these models usingVHDL and analysed the results through simulation using Xilinx ISE.

Index Terms – Array Multiplier, Vedic Multiplier, Reversible logic gate, Floating point numbers, VHDL

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INTRODUCTION

In today's modern world, the dissipation of power is the main problem. Information will be lost due to power dissipation. This happens in poor technology based on non-reversible hardware. By changing each input to a successive output, power dissipation in the digital circuit increase, through that connection increasing the loss of information. At the same time, heat generated by increasing the leakage power, due to this heat, the information loss is very high even at room temperature, the heat dissipate will be large that affecting performance, resulting in components with a shortened lifespan. Gordon. E. Moore et al. (1965) predicted that the number of items on a chip would double every 18 months. Looking closely at the effects of Moore's Law, the researchers concluded that as the number of items in a chip increases, so does the power dissipation. It also assumed that the amount of energy dissipated will be equal to heat dissipated by built devices. Considering with this in mind, reversible logic becomes a promising energy saving solution. Reversible logic circuits are seems to more power efficient than precision multipliers. By relaxing precision requirements, circuit complexity can be greatly reduced, latency, and area and power consumption. In our project comparing the 32-bit conventional Vedic multiplier and Array multiplier with the 32-bit Array multiplier and inverse logic gate for Vedic multiplier used in full adder and half adder circuits in partial product part for better performance and energy efficiency can be obtained. Traditional methods use full adders and half adders to generate multipliers that increase complexity, area, and gate-level power consumption. The single-precision floating-point format uses 32-bit computer memory and can represent a wide variety of values. Commonly mentioned to as FP32, this format is best used for calculation that doesn't hurt without a bit of approximations. Single precision binary IEEE 754 representation format contains a one-bit sign (S), an eight-bit exponent (E), and a twenty-three-bit fraction (M) or mantissa, in our project we are used logic reversible gates in mantissa multiplication part, exponent part and in sign bit part also we used logic reversible gate with this we obtained reduced power consumption and efficiency in performance compared to the conventional single precision floating point.

II. DEFINITION OF REVERSIBLE LOGIC:

This section describes some important aspects of reverse logic. The main purpose of the reverse logic theory is the inverse function, which is defined as follows.

1. Reversible Function:

   A Boolean function f(x1, x2 … xn) of n Boolean variable is called a reversible Function if:

   1. The number of outputs equals the number of inputs
   2. Pattern of Any output is mapped to a single input pattern

That is, a reversible function is functions that allow groups of input vectors [7-9]. For a function (n, k), that is to say a function with n inputs and k outputs, it is necessary to add an input or output to make reversible. This leads to the following definitions.

2. Reversible logic gate:

The number of outputs of a reversible valve is equal to the number of inputs, and there is a one-to-one correspondence between input vectors and output vectors [10-12]. This not only helps to identify outputs from inputs, but also helps to unambiguously extract inputs from outputs.

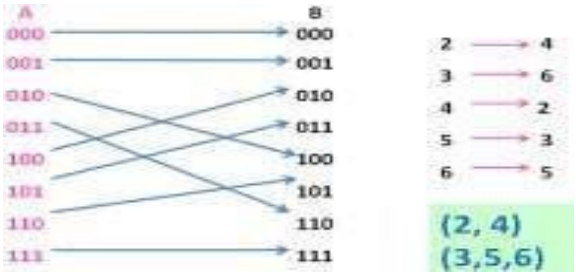


Figure 1: Reversible Logic implementation Example

REVERSIBLE LOGIC GATES:

In this section we will explain all about reverse logic gates. Although spurious outputs are briefly described, in this section we describe them using more appropriate logic gates.

1. Feynman Gate:

Let Iv = (A, B) and Ov = (P = A, Q = A ⊕ B), where Iv and Ov are the input and output vectors of 2 x 2 Feynman gates (FG) [3] respectively. A block diagram of a 2x2 Feynman gate is shown in figure 2

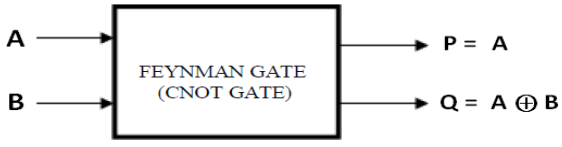


Figure 2: 2*2 FEYNMAN GATE

2. Peres Gate:

Let I_v= (A, B, C) and O_v = (X=A, Y=A⊕B , Z=AB⊕C), where Iv and Ov are the input and output vectors of 3 x 3 Peres gate (PG) [3] respectively. A block diagram of a 3x3 Peres gate is shown in figure 3

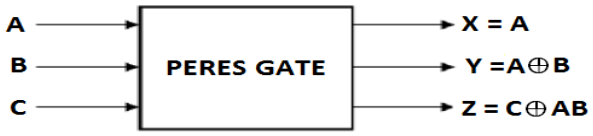


Figure 3: 3*3 PERES GATE

3. Toffoli Gate:

Let I_v = (A, B, C) and O_v=(P=A, Q=B, R=AB⊕ C), where Iv and Ov are the input and output vectors of 3 x 3 Toffoli gate (TG) [3] respectively. A block diagram of a 3x3 Toffoli gate is shown in figure 4

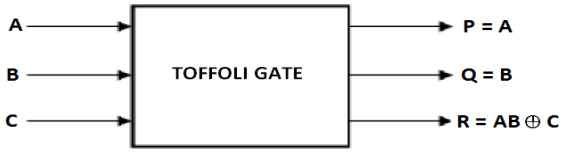
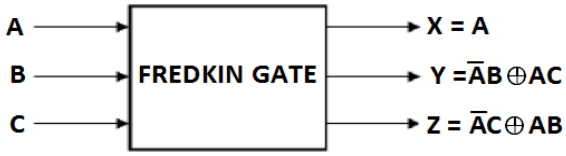


Figure 4: 3*3 TOFFOLI GATE

4. Fredkin Gate:

Let I_v = (A, B, C) and O_v = (X=A, Y=A'B⊕AC, Z=A'C⊕AB), where Iv and Ov are the input and output vectors of 3 x 3 Fredkin gate (FG) [3] respectively.



A block diagram of a 3x3 Fredkin gate is shown in figure 5

Figure 5: 3*3 FREDKIN GATE

III. METHODOLOGY

The product of an n-bit multiplier and an m-bit multiplicand, and the product are represented by an n + m bit binary number. Partial product can be added sequentially or using a series of parallel adders would be used to complete the equation. The circuit is combinational because its output depends only on its current inputs; this process is called as array multiplication. Vedic mathematics is ancient mathematics which is more effective than other mathematical techniques. Vedic mathematics is used in many applications such as arithmetic operations, number theory, compound multiplication, squares, cubes, square and cube roots, etc.

There are 16 sutras and 14 sub-sutras in vedic mathematics. Among these scriptures, only three scriptures and two subparts are used for multiplication. Urdhva-Triyagbhayam is a universally accepted method of all multiplications. In our project comparing the 32-bit conventional Vedic multiplier and Array multiplier with the 32-bit Array multiplier and inverse logic gate for Vedic multiplier used in full adder and half adder circuits in partial product part for better performance and energy efficiency, compared to the traditional method.

The single-precision floating-point format uses 32-bit computer memory and can represent a wide variety of values. Commonly referred as FP32, this format is best used for calculation that doesn't hurt without a bit of approximations. Single precision binary IEEE 754 representation format contains a one-bit sign (S), an eight-bit exponent (E), and a twenty-three-bit fraction (M) or mantissa, in our project logic gates reversible are used in mantissa multiplication part, exponent part and in sign bit part also we used logic gates reversible with this we obtained reduced power consumption compared to always having a floating point single precision.

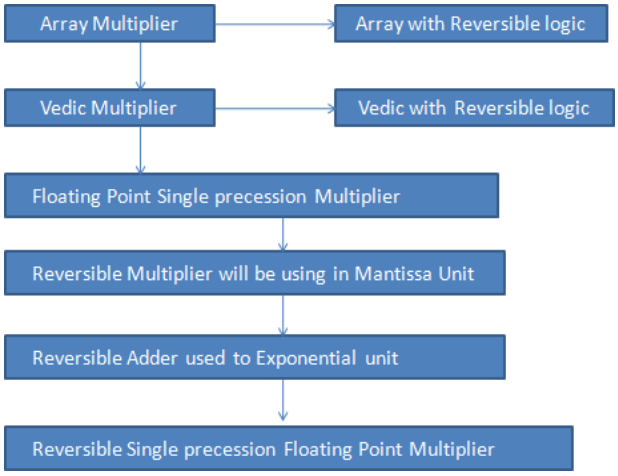


Figure 6: Methodology

IV. PROPOSED WORK

4.1 Array Multiplier using reversible logic:

The product of an n-bit multiplier and an m-bit multiplicand, the product is represented with an n + m bit binary number. To complete the multiplication, the partial products can be added sequentially or the partial products can be added by parallel half adder and full adder designed using reversible logic gates such as Fredkin, Feynman, Toffoli and (PG) Peres gates. Figure.7 shows example of 4x4 array multiplier using reversible, which is considered for a design of 32-bit reversible logic for array multiplication.

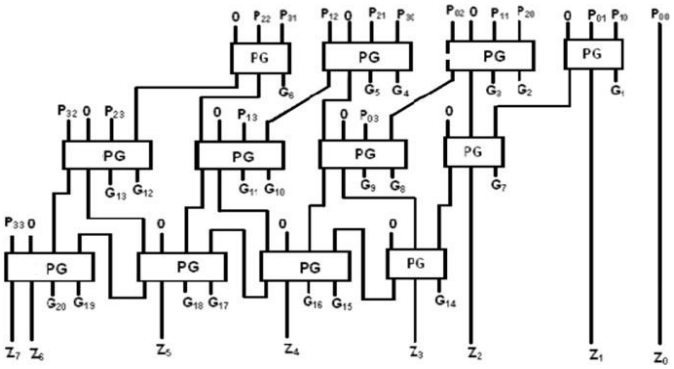


Figure 7: 4x4 reversible logic for array multiplication

4.2 Vedic multiplier using reversible logic:

A 2 x 2 Urdhva Tiryagbhyam multiplier using traditional logic will have 4 outputs. The explanation is given below.

q0= a0.b0
ql= (a1.b0) xor (a0.bl)
q2= (a0.al.b0.bl) xor (al.bl)
q3= a0.al.b0.bl

The reverse logic for the above requires Peres gate four and one FredKin gate. Most low-power designs today are designed using logic gates reversible because there is no internal power. Figure.8 shows the example of logic reversible implementation for 2x2 UT multiplier, which is considered in our design of 32-bit reversible logic for vedic multiplication.

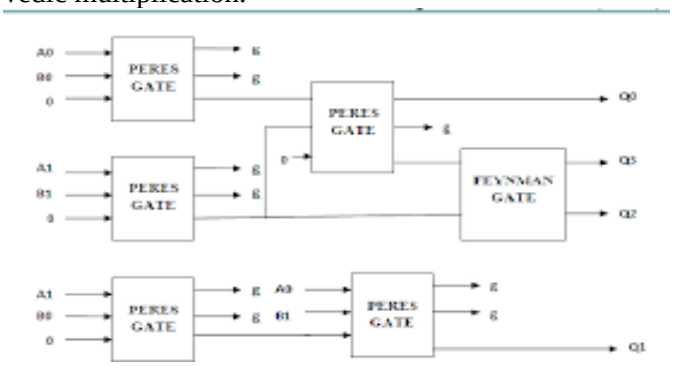


Figure 8: 2x2 reversible logic for vedic multiplication

4.3 Floating Point Multiplier using reversible logic:

This multiplier is often used to multiply two floating point numbers. A separate algorithm required to balance these numbers. Particularly if we use 32 bits versus 64 bits input, multiplication here is easier than adding.
One way to represent real binary numbers is in floating point format. There are two different types of IEEE 754 standard. Binary Exchange and Decimal Exchange Format The dynamic range in multiplication floating point is wide, which is useful in DSP applications. This article focuses only on the single

precision normalized binary exchange format. The figure below shows the IEEE 754 single-precision binary format representation; has a one-bit sign (S), an eight-bit exponent (E), and twenty-three decimal numbers (M or mantissa). Add a little more to the fraction to make what is called a mantis 1. If the exponent is greater than 0 and less than 255 and the value's MSB has 1, it is said the number is normalized. In this design, the mantissa multiplier is used by the inverse logic gates. We need an adder to create a set of multipliers, because multiplication will add. This is why multipliers are created with half and full adders. This inner content is known by the Peres gate (PG) and other reverse gates.

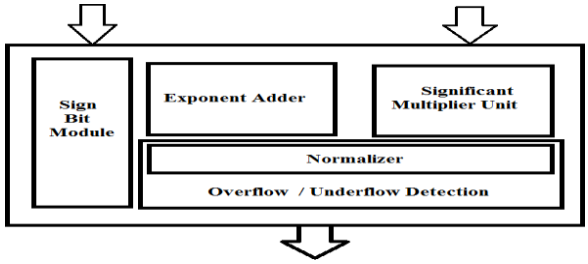


Figure.9: Block diagram of FP Multiplier

4.4 PROCESS:

As mentioned in the introduction, a normalized floating-point number has the form

Z= (-1S) * 2 (E - Exponent) * (1.M).

To multiply two different floating point numbers, follow this step:

1. Multiplying the significant; i.e. (1.M1*1.M2)
2. Decimal point position in result
3. Adding the exponents; i.e. (E1 + E2 – Bias)
4. Obtaining the sign; i.e. S1 xor S2
5. Normalization of results; i.e. getting 1 at the MSB of the results‟ significant”
6. Rounding the result to match the available bits
7. Checking for overflow and underflow occurrence

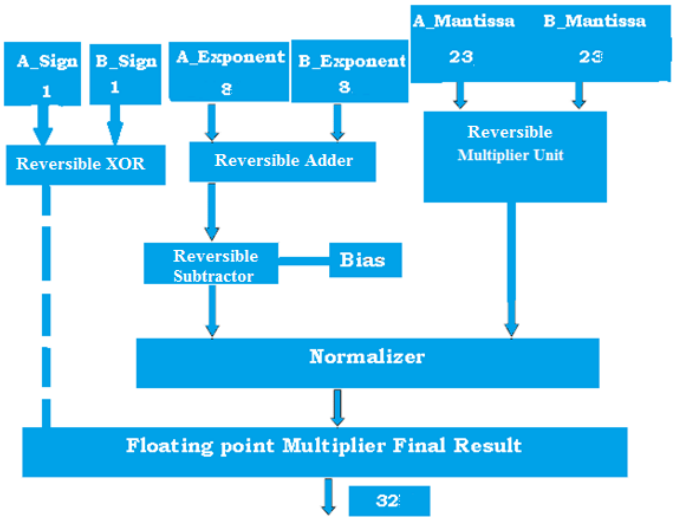


Figure.10: Proposed Diagram

V. RESULT AND DISCUSSION

5.1 Reversible logic for array multiplication:

The proposed 32-bit array multiplier designed using reversible logic. The simulation is performed by using Xilinx ISE 14.7.Figure.11 shows the simulation results.

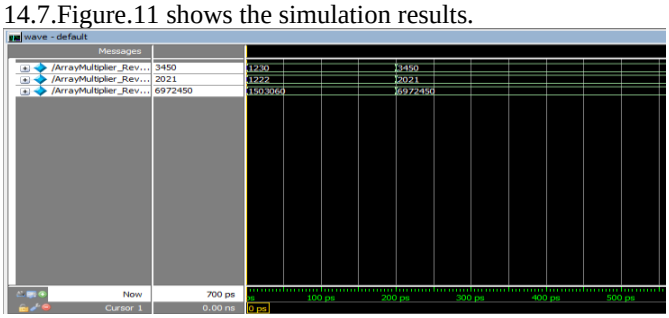


Figure.11: Output wave form of proposed reversible logic for array multiplication

The above figure.11 describes the output waveform of 32-bit reversible logic for array multiplication method for the given hexadecimal input values a= 3450 and b= 2021 and product of these values, it is modelled using verilog code and the output result of value Y= 6972450 is observed.

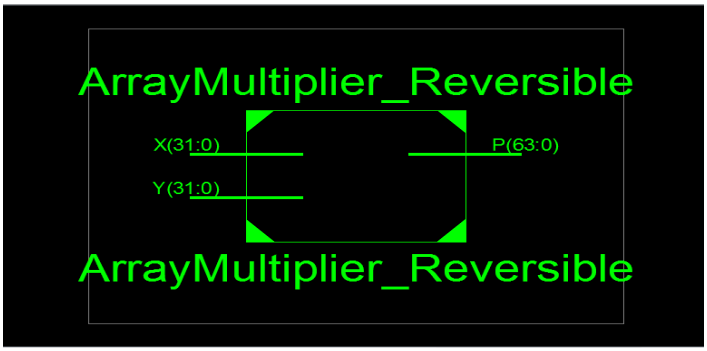


Figure.12: RTL Diagram of reversible logic for array multiplication

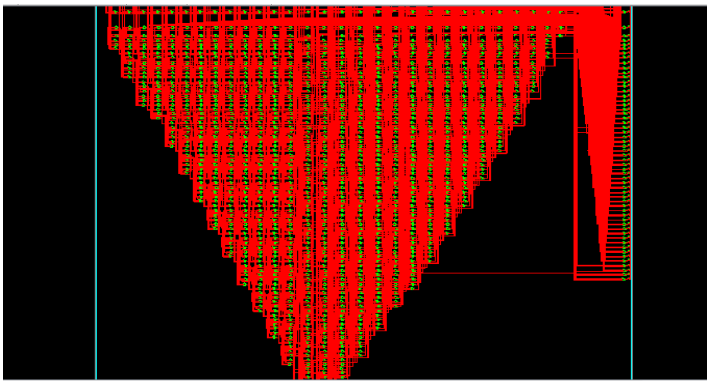


Figure.13: Technology Diagram of reversible logic for array multiplication

Above figures 12 and 13, represents the RTL diagram, Level 1 schematic and Technology diagram of proposed 32-bit reversible logic for array multiplication method.

5.2 Reversible logic for vedic multiplication:

The proposed 32-bit using reversible logic Vedic multiplier designed. The simulation is performed by using Xilinx ISE 14.7.Figure.14 shows the simulation results.

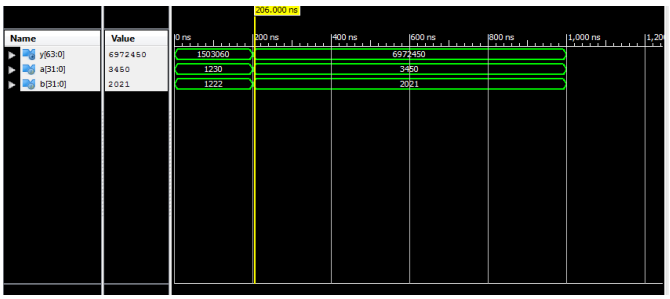


Figure.14: Output wave form of proposed reversible logic for vedic multiplication

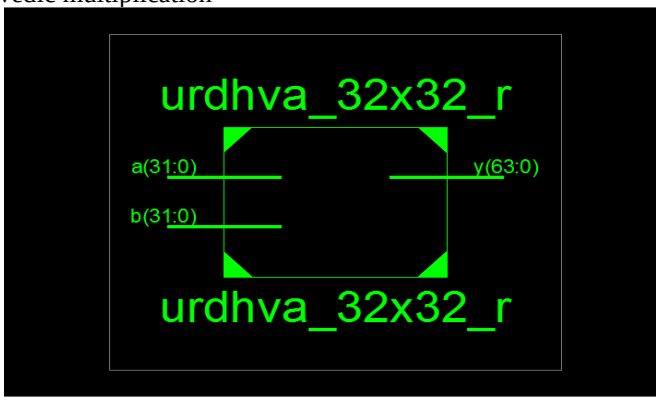


Figure.15: RTL Diagram of reversible logic for vedic multiplication

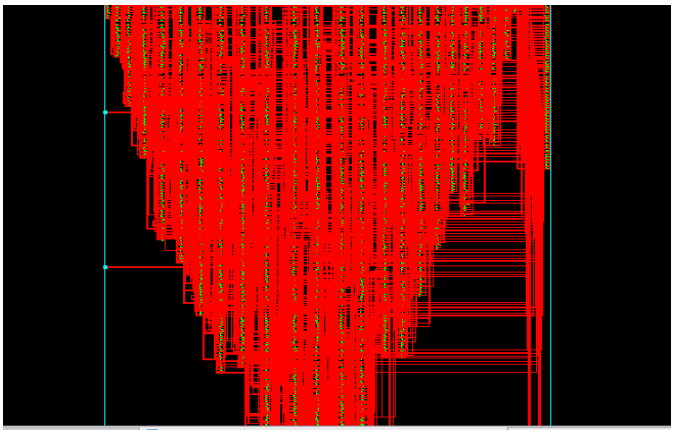


Figure.16: Technology Diagram of reversible logic for vedic multiplication

Above figures 15 and 16, represents the RTL diagram, Level 1 schematic and Technology diagram of proposed 32-bit logic reversible gates for vedic multiplication method gates.

5.3 Reversible logic for Floating Point Multiplier:

The performance of proposed floating point single precision multiplier using logic reversible gates is validated using Xilinx ISE 14.7. Fig. 5.3.1 shows the simulation of proposed floating point single precision multiplier using reversible logic gate.

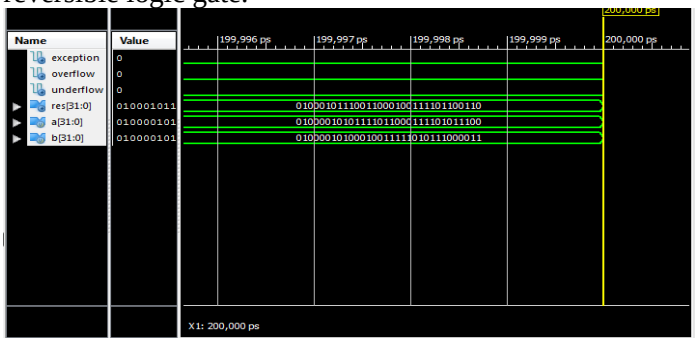


Figure.17: output waveform of reversible logic for FP multiplier

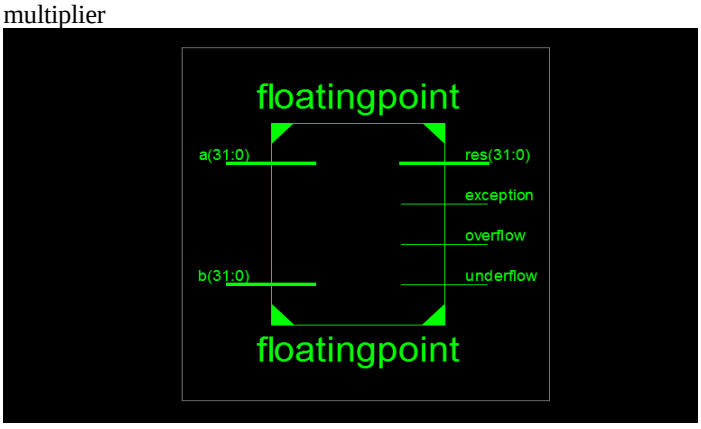


Figure.18: RTL Diagram of reversible logic for FP multiplier

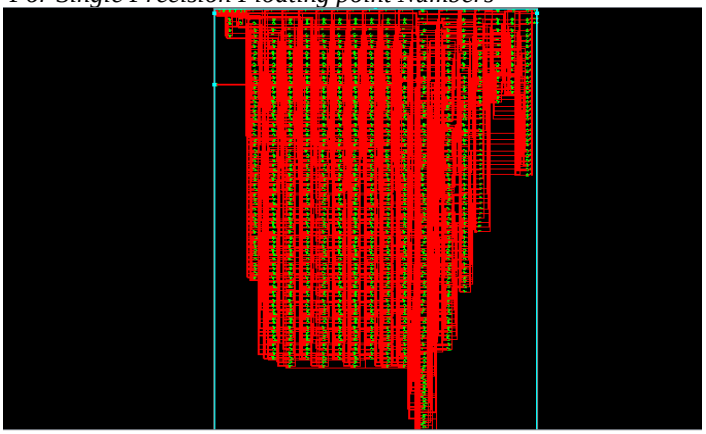


Figure.18: Technology Diagram of reversible logic for FP multiplier

Above figures 18 and 19, represents the Level 1 schematic diagram and Technology diagram of proposed 32-bit floating point multiplier for single precision using reversible logic gates. The performance of instruction array reversible logic multiplier, Vedic reversible logic multiplier and floating point numbers using reversible logic gates are evaluated in terms of power, delay and area of the designed circuits. The proposed design is compared with conventional Array multipliers, Vedic multipliers and floating point numbers with the above proposed design. The proposed reversible design concept was implemented using Xilinx ISE 14.7 tools.

Table-1: Power, delay and area of the proposed reversible logic multiplier

Modules	**Power** (mW)	**Delay** (ns)	**Area** (LUT)
Array Multiplier	43.61	92.08	1428
array Multiplier using reversible logic	16.07	92.75	1439
Vedic Multiplier	45.61	68.89	1654
Vedic Multiplier using reversible logic	16.07	68.03	1928

Table 1 shows the comparison of conventional array multiplier and vedic multiplier with proposed array multiplier and vedic multiplier using reversible logic. It reduces power, latency and efficiency respectively compared to traditional multiplier designs.

Table-2: Power, delay and area of the proposed floating point multiplier using reversible logic

Modules	**Power** (mW)	**Delay** (ns)	**Area** (LUT)
Floating point unit	36.14	27.63	90
Floating point unit using reversible logic	26.79	85.97	860

A high performance 32-bit reversible floating point single precision multiplier unit for DSP applications is proposed, designed and implemented according to the IEEE 754 standard. A floating point single-precision multiplier using reversible logic unit is used for FIR filtering applications. Simulation results and comparison studies with existing floating point multiplier unit modules show that the proposed module has high computational performance and low power consumption.

VI. CONCLUSION

Reversible logic gates store information during calculation, thus offering a compact design for low power consumption. While reverse logic circuits try to minimize data loss, they can push the limits of low power consumption. This article presents a performance-saving array multiplier, Vedic multiplier using reversible logic, and a 32-bit single precision floating point multiplier using reversible logic gates for signal processors application. Compared with the existing traditional array, vedic multiplier and floating point multiplier designs, the concept of reversible array multiplier, vedic multiplier and floating point multiplier design has the advantage of low power consumption and high performance. Using another method, this model can be further optimized in terms of delay, power, area of proposed design and accuracy of the result can be increased this can be regarded as future scope of this project.

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