ISSN 2063-5346

# ETHERNET MAC CORE USING VERILOG

**Shilpa K. C[1],Anusha. H[2], Bhoomika K. R[3] and Pavithra .S[4]**

[1,2,3,4] *Dr.Ambedkar Institute of Technology,India*

*Department of Electronics and Communication*

E-mail:shilpa.kc2@gmail.com

**Article History: Received:** 12.05.2023 **Revised:** 25.05.2023 **Accepted:** 05.06.2023

**Abstract**

*As there is a development in the technology and the number of users on the internet are growing, so there's a want for the quickest transmission of the data among the users.. Communication among the customers isn't as easy as it happens; it entails many history hardware components, protocols and strategies to be undertaken. For instance, a go with the drift net from the server room to the gadgets pass through firewalls, routers, switches and a few passive community factors and most of these are interconnected through the wires can be a twisted-pair or an optical fiber cable through the connectors and a trans receivers. In our project we're designing a Mac Core that enables to transmit the data at a higher rate with the help of specific ranges of frequency i.e., 10Mhz, 100Mhz and 1000Mhz with the usage of a simulation tool that enables to transmit the frames or packets on the information data link layer and particularly right here we're implementing the speed of 2.5gbps and more using the tri mode levels.*

***Keywords:****Ethernet, Interfaces, Pause Frames, CRC, EDA Tool*.

## 1.INTRODUCTION

While the first version of the technology only had a speed of 3 megabits per second, Ethernet protocol today enables speeds of up to 1000 megabits per second. Earlier Ethernets were limited to a building, but today Ethernet can cover a range of just over 6 miles with the use of fiber optic cables. Over the course of its development, Ethernet has taken over a dominant role among LAN technology and outperformed various competitors. In addition, today real-time Ethernet is the industry standard for communication applications.

The generation made a vast contribution to the manner for the improvement of the Ethernet each year. We can see the evolution of Ethernet that has took place and could show up in future. Today, the widely-disbursed IEEE standard 802.3 is utilized in offices, personal households, server and manipulate rooms, communique networks, mobile networks and so on.

Ethernet become evolved in 1973 through Bob Metcalfe on the Xerox Palo Alto Research Center in California and supported via way of means of thick copper coaxial-kind cables. The first version, 10BASE5, featured extraordinarily stiff cable almost a 1/2 of-inch in diameter, and then we had 10BASE2 which was about half as thick and much more flexible than the first. In the past 1980s, the improvement of the Ethernet hub, and later

the switch, allowed twisted-pair copper cables to come to be the number one medium for the aid of Ethernet.

Xerox collaborated with different vendors-Digital Equipment Corporation and Intel to release the primary 10 Mbps Ethernet specification in 1980 and thereafter the IEEE standard committee was formed to set an open standard for the Ethernet Technology.

## 2.PROBLEM STATEMENT

Ethernet is much less at risk of disruptions compares to WLANS. It can provide an extra diploma of community safety and it makes tough for outsiders to get entry to information or hijack bandwidth for unsanctioned devices. Wired Ethernet connections are faster, extra reliable, and decrease latency than Wi-Fi connections. Even though more recent Wi-Fi requirements like Wi-Fi 6 have made their way to the market but when overall performance is a priority, Ethernet makes an impact.

## 3. OBJECTIVES

The main objective of this paper is:

- To design an Ethernet MAC CORE using tri modes i.e.,10/100/1000 MHz on an EDA (Electronic Design Automation) platform and code implementation to operate in three different ranges using a Verilog hardware programming language.
- Toincreasetheperformanceofspeedrange upto2.5Gbps and more using these three ranges of speed as the base.

## 3.1.RELATEDWORKS

### PAPER1:Trimodefull-duplexMACinVHDL

This paper was published in the year 2018 by Dr.Rajendra Varma PS, Kulkarni Srivathsav.

This paper gives an overview of the features and usage of the MAC and provides a source code for thedesign of Ethernet MAC using VHDL on the Xilinx software platform and it highlights almost all thecommandsand theirrespectivedescription makingus possibleto understand in a better way.

### PAPER 2: Triple-Speed Ethernet Intel FPGA User Guide

This paper was published in the year 2020 and is presented by Intel.

This paper gives an overview Presents the information about the MAC architectures and the interfaces involved in the Ethernet and also some of the test bench and simulation models and results which helped us to know the inner functionality involved within the Ethernet.

## 3.2 SPECIFICATIONS

Ethernet Mac Core block diagram is in the upcoming page and according to that block diagram we have to write the code in Verilog in the EDA playground. For every single block the code is separately written and then the functions are interlinked and called in the top module of the code. When the code is simulated in the EDA playground we can obtain the waveforms which show the clock frequency generation wave for configured value and the wave which shows the data transmission required speed rate.

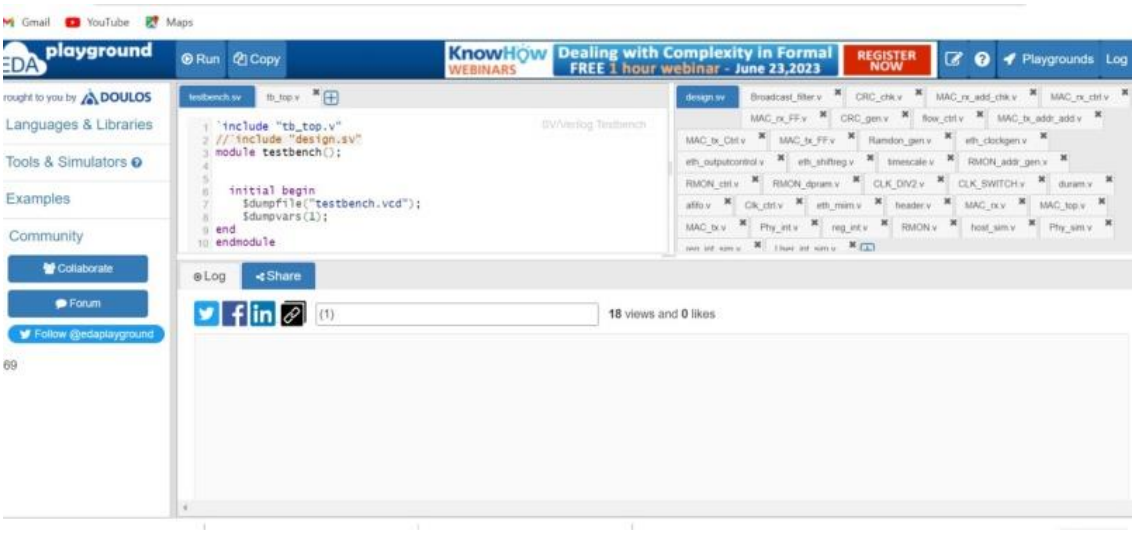


Fig.1.Code implementation on EDA Playground.

## 4.METHODOLOGY

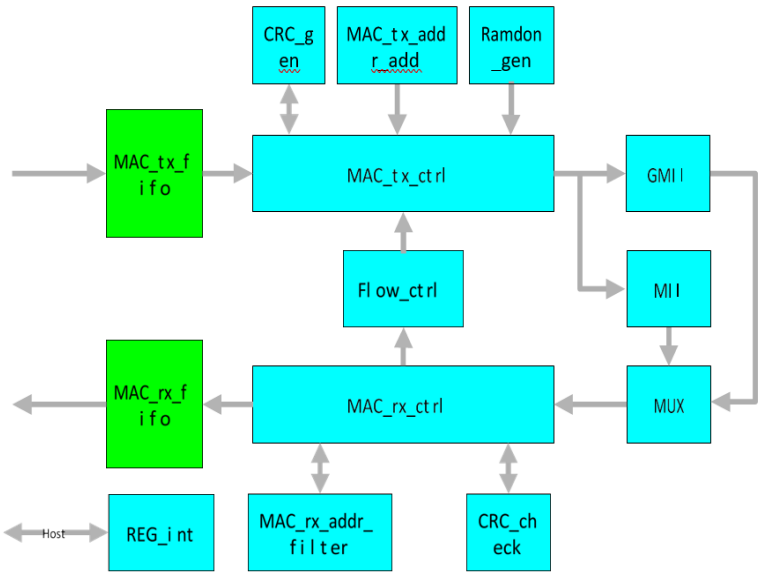


Fig.2.Block diagram of Ethernet MAC Core.

Descriptions of the practical blocks and interfaces are mentioned below:

- **The client interface**: It is designed for maximum flexibility in matching to a switching processor interface. This interface tries to map the transmitter and receiver processor in order to match them for proper transmission.
- **Transmit Engine**: The transmit engine takes information from the client and converts it to Ethernet format. Preamble and CRC fields are added and the data is padded if necessary. The transmit engine additionally offers the transmit data vector for every packet and transmits the pause frames generated through the flow control module.
- **Flow Control**: The MAC may be configured in such a way that the transmitter can hold the frames for specified amount of time when the receiver is not in the position to

receive the frames. It helps lossless transmission.

- **GMII/MII Block**: The Gigabit Media Independent Interface (GMII) will be used if the speed requirement is in terms of GBPS and Media Independent Interface (MII) will be used if the speed requirement is in terms of MBPS
- **MDIO Interface**: The optional MDIO interface may be written to and examine from the use of the Management Interface. The MDIO is used to reveal and configure PHY devices. The MDIO Interface is described in IEEE 802.3 clause 22.
- **Address Filter**: This block functionality is almost similar to the functionality of the firewalls where we can specify some host addresses and if the frames or packets come from these addresses then those frames or packets will be filtered.
- **A cyclic redundancy check (CRC):** It is an error-detecting code typically utilized in digital networks and storage devices to hit upon unintentional changes in the received digital data. Blocks of information coming into these structures get a short check value,
- this check value gets appended with the transmitted data and at the receiver side, when the information is received again the short check value will be computed. Both the check values are compared if same then the information is not corrupted
- **First in first out (FIFO**): It is a type of file that will allow communicating many independent processors. One FIFO file will be opened for writing while the other will be for reading after which data can flow as usual.

## 5.FEATURES

- Designed to IEEE 802.3-2012 specification.
- Supports 10/100/1000/2500 Mbps Ethernet.
- Configurable half-duplex and full-duplex operation.
- Concept of flow control enables lossless transmission.
- Optional MDIO interface to control in PHY layers.
- Optionalclockenablesto reduce clockusage.
- SupportofVLANframestospecification *IEEE802.3-2005*.
- Optionaladdressfilterblock for enhanced security.
- Configurable support forjumbo frames ofanylength.

## 6. RESULT ANALYSIS

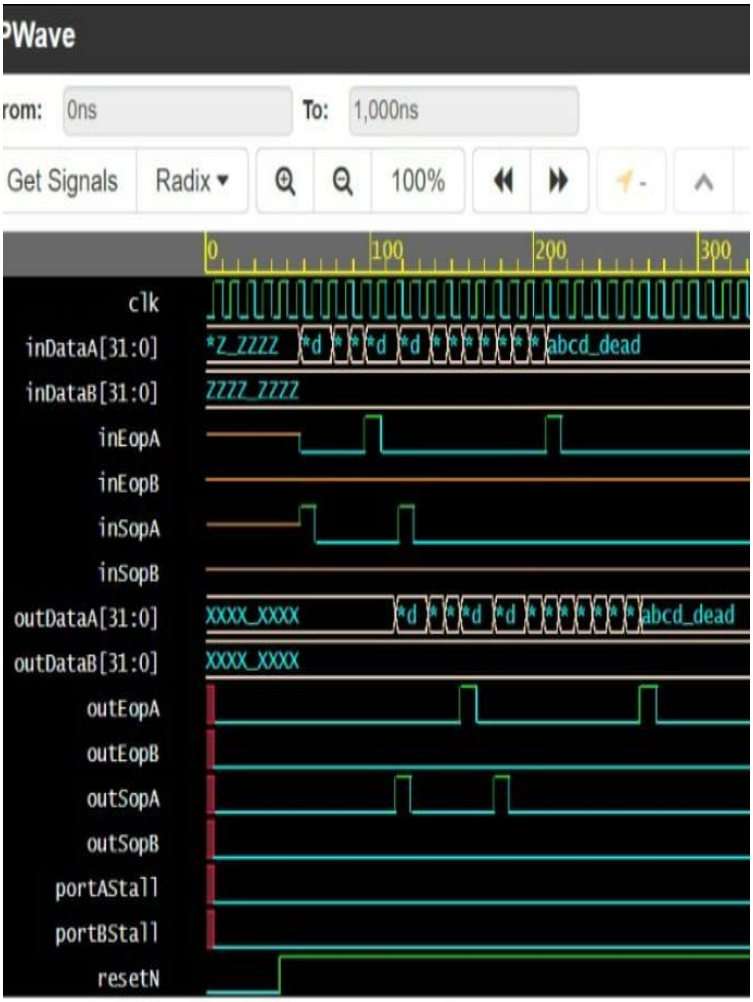


Fig.2.Graph representing the speed configuration of Ethernet mac core

The above waveform consists of input data, start of packet A, end of packet A, start of packet B, end of packet B, but here we are sending packets only in A. The positive edge of packet A represents the start of packet and the negative edge represents the end of packet. So the number of cycles in between start of packet and end of packet is 4 clock cycles. Here 1 clock cycle=1ns hence 4 clock cycle =4ns, and since 1ns=1000 MHz here we are sending a packet at a speed of 4000 MHz This speed was achieved with the help of tri modes (10/100/1000). For thisimplementation we took 10 MHz as a reference.

**Calculation:**

**(**f/2)*100=(10/2)*100=500MHz

500 MHz /125 MHz=4ns

Here 125 MHz is the clock divider used in order to divide theclock to reduce the traffic in between the packets.

## 7. CONCLUSION

Ethernet being a part of the whole network communication system and playing an important role in the transmission and reception of the information its necessary to know about it in detail and to makeattempts for implementing the Ethernet with respect to its standards is necessary.

Ethernet has advanced from 10Mb/sec to 400G and could visit 800G or likely 1 terabyte Ethernet with the aid of using approximately 2030, in line with the

roadmap.5Gmobiledeploymentisdrivingdramaticincreasesvarious applications, which continue stopush Ethernet requirements for high errates and longer distances.

## REFERENCES

[1] *IEEEStandard802.1Qbb,*"IEEEStandardfor Local and Metropolitan Area.

[2] *VivadoDesignSuite:DesigningIPSubsystemsUsing IPIntegrator*(UG994)

[3] *AXI1G/2.5GEthernetSubsystemProductGuide* (PG138)

[4] *AMBAAXI4-StreamProtocolv1.0Specification*(Arm IHI0051A)

[5] *IEEE802.3-2008specification*

[6] *1G/2.5GEthernetPCS/PMA*or*SGMIILogiCOREIP ProductGuide*(PG047)

[7] *7SeriesFPGAsClockingResourcesUserGuide* (UG472*)*

[8] *VivadoDesignSuiteUserGuide,DesigningwithIP* (UG896)

[9] *VivadoDesignSuiteUserGuide:GettingStarted* (UG910)

[10] *VivadoDesignSuiteUserGuide:UsingConstraints* (UG903)

.