Section A-Research paper

Highly efficient GDI Technique used to implement 1 bit ALU

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Abstract

It uses distributed gate entry technology to reduce power dissipation and leakage current. Space, latency and performance are also optimized using this. Used in this research paper to use different types of multiplexers and 1-bit ALUs. Here use cadence virtuoso 4.1 software to know.

In GDI technology, there is 82% advantage in current flow, 76% in power distribution, and 74% in gates. This technology has the advantage that it is not difficult in logic circuit design. This article shows a comparison with standard CMOS and GDI designs.

Keywords: Dynamic power dissipation, Leakage current, GDI technique, Area optimization, VLSI.

I. INTRODUCTION

The use of portable digital notebooks has led to many studies such as the need for speed, optimization and low power consumption [1]. The improved performance of logic circuits, once based on CMOS standards, has led to many advances in logic design over the past two decades. A popular form of logic in low voltage electronics is pass transistor logic (PTL).

announced nMOS, derived from transistor logic. They follow a pattern in which the control signal is applied to the gate of the n transistor.

Instead of n transistors, another set of data signals is used [1].

Many practical PTL applications have been reported in the literature [2,3,4,7]. The advantages of the

PTL over the standard CMOS design are: High speed - due to small capacity size; Low power consumption - due to the reduced number of transistors; The effects are lower [5,6] - due to the smaller area. There are two main problems with using the

PTL. First, the lower value of the single-channel pass-through transistor results in less driver current and hence slower operation of the reduced power supply; this is especially important for low-power designs where the lowest possible performance is desired.

Second, direct power distribution will be important, as the regenerative inverter has no "high" voltage input level Vdd, so the PMOS device in the inverter is not completely shut down [3]. Another problem with current PTLs for the

is the complexity of the top-down process, which prevents the transistor from playing a significant role in the actual logic LS1. One of the main reasons for this is the lack of simple libraries and target cells for PTL-based design. A new low power generation technique, GDI (Gate Diffused Input Technology), which can solve most of the above problems, is proposed in [9]. The GDI approach allows many complex functions to be implemented using only two transistors.

This approach is suitable for fast, low-power, low-power electronics while improving power characteristics (compared to current CMOS and PTL technologies) and allows easy Shannon theorem-based design using mobile phones. libraries [9].

The purpose of this study is to analyze GDI technology using logic gates and compare its properties with its analogues in CMOS. To demonstrate the effectiveness of GDI and demonstrate its properties, production relied on technically borrowing GDI and CMOS cells.

II. BASIC GDI FUNCTIONS

Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions.

The GDI method is based on the use of simple cells as shown in Figure 1. At first glance, the basic cell is reminiscent of a standard CMOS inverter, but there are some key differences: the GDI cell has 3 inputs - G (input gate for input gate) nMOS and PMOS), P (source/drain for PMOS input) and N. (nMOS). source/pool input). It should be noted that not all tasks can be done in p-well CMOS process,

but can be done in double-well CMOS or SOI technology.

Table 1 shows how a simple change in the input configuration of a simple GDI volume corresponds to various Boolean properties.

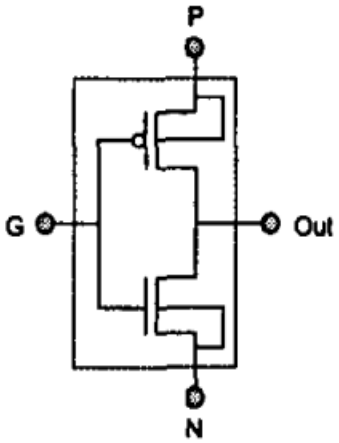


Fig 1. GDI basic cell

Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

Table 1. Various logic functions of GDI cell for different input configurations

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

GDI has some important features that can improve the design of complex stages, the number of transistors, static electricity, and logic stage oscillation. Understanding GDI volume features requires in-depth functional analysis of the base volume under different conditions and configurations.

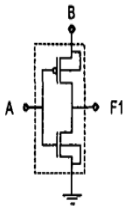
III. OPERATIONAL ANALYSIS OF GDI CIRCUITS

One of the common problems in PTL design is low output oscillation caused by the initial loss of the pass transistor. An additional connection is used to solve this problem in current PTL technology. To understand the impact of low-level issues in GDI volumes, we recommend the following analysis as an example of the F1 function and can be easily extended for use in other GDI projects. Table 2 lists all logic states and their effects on the operation of F1.

It can be seen from Table 2 that only A = 0 and B = 0 are the cases where the output value has low oscillation.

In this case, the voltage level of F1 is VTp (change from expected 0V) due to the negative transition of the PMOS pass transistor [4]. Apparently, the only case where this phenomenon occurs (among all possible changes) is the transition from A = 0, B = VDD to A = 0, B = 0. %; in this case (for B = 1) the GDI cell operates as a regular CMOS inverter, which is commonly used as a digital buffer for logic level recovery. In some of these cases, when VDD = "1" and there is no loss of oscillation in the previous phase, the GDI unit operates as a negative inverter and restores the oscillating voltage. Although this feature allows for self-oscillation in some cases, this article assumes the worst case and uses additional electronics in the power supply for oscillation.

Table 2. Input logic states vs. functionality and output swing of F1 function.



A	B	Functionality	F1
0	0	*pMOSTrans Gate*	V_{Tp}
0	V_{DD}	*CMOSInverter*	V_{DD}
V_{DD}	0	*nMOS Trans Gate*	0
V_{DD}	V_{DD}	*CMOSInverter*	0

IV. COMPARISONS WITH CMOS LOGIC

The simulation of the 1 bit ALU is shown in figures.

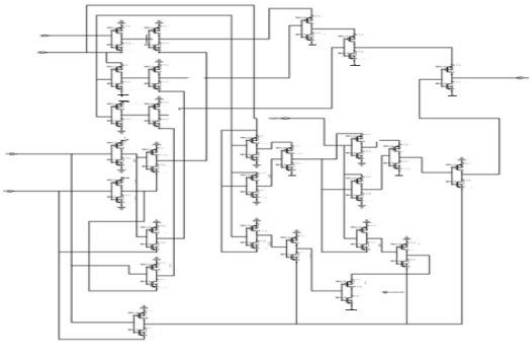


Figure 2.Transistor level representation of 1-BIT ALU with GDI technique

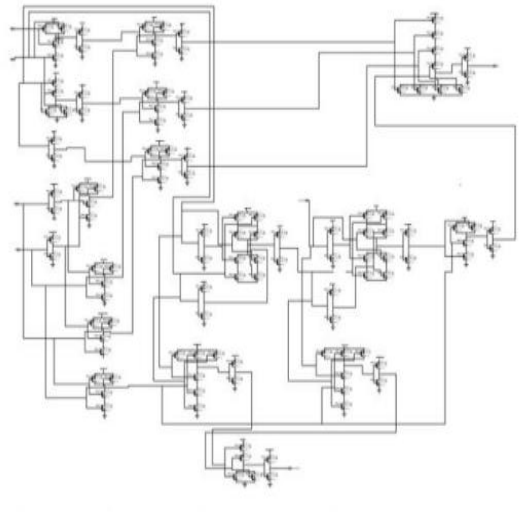


Figure 3.Transistor level implementation of 1 BIT ALU with CMOS technique

Table 3 COMPARISION BETWEEN GDI AND CMOS

Device	No. of Transistor in CMOS	No. of Transistor in GDI
1 bit ALU	118	54

TABLE –4 SIMULATION RESULT IN TERM OF LEAKAGE CURRENT

Device	Leakage current in CMOS	Leakage current in GDI
1 bit ALU	8.18ma	3.57ma

TABLE –5 SIMULATION RESULT OF IN TERM OF DYNAMIC POWER CONSUMPTION

Device	Dynamic power consumption in CMOS	Dynamic power consumption in GDI
1 bit ALU	102.5µw	39.3µw

V. CONCLUSIONS AND FUTURE RESEARCH

Different implementations of the new gate diffused entry (GDI) technique have been proposed for low-power designs. An additional 1-bit is used for GDI and CMOS and is compared to CMOS technology in simulation. In this article, GDI has been reduced by 54% compared to CMOS, greatly improving performance and reducing the number of transistors in the GDI circuit compared to CMOS. The implementation of the
GDI circuit must provide power time due to the use of a complete cell library with a reduced transistor count. The benefits of
GDI technology, 2-transistor implementation of complex logic functions, and manual recovery of some functions are already features of the electronic design.
This, along with quality measurement and simulation results, provides evidence that the GDI design can support the VLSI designer's tool.

We hope the presented results will encourage more GDI research projects. Compatibility issues for the use of GDI for prototype design and dual quality CMOS processes are currently under investigation. Recently, much work has been done on the automation of GDI cell-based logic design methods.

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