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FIFO Structure for Router in Bi-NoC

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Abstract

This paper describes features of a network on infrastructure in System on Chips (SoCs) as traditional methods exhibit severe bottlenecks at intercommunication among processor elements. However, designing a NoC is highly complex due to a number of factors There are a number of issues concerning the performance metrics of system scalability, latency, power consumption, and signal integrity in routers. This paper discusses the memory unit in routers and proposes a more advanced memory structure.comparing the simulations and synthesis results to previous walls, guaranteed throughput. Comparing the simulation and synthesis results to provide works, guaranteed throughput predictable latency, and uniform network access are highly provided.

Keywords— Bi-NoC; FIFO; Virtual Channel; Switch Allocator; Router; SoC

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1.INTRODUCTION

Field programmable gate arrays (FPGAs) provide high performance for real-time applications in one in all the fastest growing industries However, the scale and loss in yield are increasing with decreasing channel length of CMOS. Moore proposed that the number of devices in system is double at every eighteen months therefore concentrating on different aspects while designing applications supported VLSI technology. To accommodate higher operating frequencies with the increasing transistor density, and shorter time-to-market pressure, chip multiprocessor (CMP) and multiprocessor system on chip (MPSoC) architectures are proposed Bus structures for on-chip communication and combined complex heterogeneous functional devices on a single chip are more and more required in today's semiconductor industry. The traditional intercommunication architectures are unable to supply huge performance in case of MPSoC and CMP (1) Network-on chip (NoC) is one of popular solutions for the issues of intercommunication among processing elements (PEs) in systems on chip (SoC) Using NoC as tool for intercommunication for FPGAs isn't a replacement idea, whereas the existed interconnecting methods like crossbars exhibit poor scalability therefore the development of new NoC architectures are the most effective suited to FPGA [2] Designing of new NoC architecture is still a challenging problem for researchers to realize high performance without sacrifice of speed and throughput NoC is the term mentioned to explain an intercommunication architecture that is maintaining of design solutions for communication-centric trends A typical NoC architecture consists of multiple connections and various routers to transfer the info among PES INOC is framed sort of a block architecture, which configures the wires and routers like street grids, and PES are separated by wires oncity blocks but routers and PEs, Network Interface (Nl) is one of important design constraint for NoC because it transforms data packet PEs into foxed length of flow control digits (flits) The entire data packet is especially divided into three flits that are header, body and tail fit. Theses[3] are forwarded and routed with control mechanisms towards the destination through current router to neighbour routwithin the city-block based tile NoC, the router consists of five bi-directional input and output ports that are east,south, west, north and local port of associated PE To intercommunicate between the ports efficiently, each bidirectional port is connected neighbour port with set of physicalinterconnected wires: The router is known as the known as theheart of NoC because it transfers and controls the data based on various methodologies.To describe the function of router, a 5X5 crossbar switch presented [4-6]. The crossbar switch moves the data from the selected input port to output port based on control logic. An arbiter is required to select appropriate input port to transfer data depending on priority among the input ports. Hence, a typical NoC router consists of five input and out ports, crossbar switch and arbiter modules to intercommunicate with PEs. Fig. 1 described the structure of 3X3 mesh based NoC where center router consists of 5X5 bi-directional ports. Source Intellectual Property (IP) initiates the data packet transferring through NI and current router receives thereafter transfers to neighbour router which is located towards the destination IP. The routing of data packets from source to destination depends on the routing algorithm that is integrated into each router. In typical NoC, an X-Y deterministic routing algorithm that routes the data based on X and Y coordinates is used to transfer from source to destination [7]. Topology is one of the major constraints for routing algorithms because measuring the distance from the source to the destination router is quite complex in the case of routers that are not aligned properly. Most of the routing algorithms are based on mesh topology as it is simple to implement [8, 9]. Fig. 1 clearly describes the X-Y routing algorithm in mesh topology from source to destination. Source

IP measures the distance to destination in terms of number of routers and locks the path until the data packet reaches destination. The address of destination and information of intermediated routers are added to the data packet before starting data packet transfer This paper identifies the limitations of memory based NoC and examines devices that must contain SoC. The size of an FPGA is expressed in logic cells (LCs), which are equivalent to a four-input look-up table (LUT). Based on this, an advanced FIFO based memory architecture is proposed for bidirectional-channel NoC. The bidirectional channel NoC combines dynamically reconfigurable channels to improve bandwidth utilisation. Usually, NoCNoC-compatible processors are found in supercomputers' GPUs. The NVIDIA computers are mainly using NoC based processors because of their higher operating speeds. The proposed design is simulated in Xilinx 14.7 ISE and implemented on a Vertex-7 FPGA. The remaining paper is as follows: Section 2 describes related work and Section propounds the structure of an advanced NoC design with improved FIFO memory in a bidirectional NoC. Section 4 presents implementation results and discussion and finally, Section 5 concludes the paper with future work.

2.LITERATURE SURVEY

1.U.Y. Ogras and R. Marculescu, "'It's a small world after all': NoC performance optimization via long-range link insertion," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 7, pp. 693–706, Jul. 2006

In this paper, (NoCs)represent a promising solution to complex on-chip communication problems. The NoC communication architectures considered so far are based on either completely regular or fully customized topologies. In this paper, we present a methodology to automatically synthesize an architecture which is neither regular nor fully customized. Instead, the communication architecture we propose is a superposition of a few long-range links and a standard mesh network. The few application-specific long-range links we insert significantly increase the critical traffic workload at which the network transitions from a free to a congested state. This way, we can exploit the benefits offered by both complete regularity and partial topology customization. Indeed, our experimental results demonstrate a significant reduction in the average packet latency and a major improvement in the achievable network through with minimal impact on network topology.

2. L. P. Carloni, P. Pande, and Y. Xie, "Networks-on-chip in emerging interconnect paradigms: Advantages and challenges," in Proc. ACM/IEEE Int. Symp. Netw.-on-Chip, May 2009, pp. 93–102.

In this paper , communication plays a crucial role in the design and performance of multi-core systems-on-chip (SoCs). Networks-on-chip (NoCs) have been proposed as a promising solution to simplify and optimize SoC design. However, it is expected that improving traditional communication technologies and interconnect organizations will not be sufficient to satisfy the demand for energy-efficient and highperformance interconnect fabrics, which continues to grow with each new process generation. Multiple options have been envisioned as compelling alternatives to the existing planar metal/dielectric communication structures. In this paper we outline the opportunities and challenges associated with three emerging interconnect paradigms: threedimensional (3-D) integration, nanophotonic communication and wireless interconnects.

3. M. P. D. Sai, H. Yu, Y. Shang, C. S. Tan, and S. K. Lim, "Reliable 3-D clock-tree synthesis considering nonlinear capacitive TSV model with electrical–thermal–mechanical coupling," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 11, pp. 1734–1747, Nov. 2013.

In this paper ,security is gaining increasing relevance in the development of embedded devices. Towards a secure system at each level of design, this paper addresses the security aspects related to Network-on-Chip (NoC) architectures, foreseen as the communication infrastructure of next-generation embedded devices. In the context of NoC-based Multiprocessor systems, we focus on the topic, not thoroughly faced yet, of data protection.We present the architecture of a Data Protection Unit (DPU) designed for implementation within the Network Interface (NI). The DPU supports the capability to check and limit the access rights (none, read, write or both) of processors requesting access to data locations in a shared memory - in particular distinguishing between the operating roles (supervisor or user) of processing elements. We explore different alternative implementations and demonstrate how the DPU unit does not affect the network latency if the memory request has the appropriate rights. In the experimental section we show synthesis results for different ASIC implementations of the Data Protection Unit.

4. A. Ganguly et al., "Intra-chip wireless interconnect: The road ahead," in Proc. Int. Workshop Netw. Chip Architectures, Oct. 2017, pp

On-chip wireless interconnects have been proposed to provide energy-efficient data communication paths between cores in System-on-Chips (SoCs) in the multi and many-core era. Networks-on-Chips (NoCs) when interconnecting hundreds of cores consume large amounts of energy and suffer from high and unpredictable latency due to congestion at intermediate routers. Wireless interconnects alleviate this problem by providing direct single-hop links between distant cores in the chip. While various wireless NoC (WiNoC) architectures have been proposed and evaluated in the in the past decade this technology is not yet adopted in the mainstream industry. In order to benefit from the past decade of research in WiNoC designs a few important myths regarding wireless interconnects need to be dispelled while propelling the research to tangible technology transfer. In this paper several vectors that define the design space of WiNoCs will be identified while highlighting the state-of-the-art accomplishments in those directions by leading research groups. This will be followed by identifying the future direction that needs to be pursued to make WiNoCs a mainstream reality. At the end a few potential high-impact use-cases for wireless interconnects are discussed.

5. B. Wu, J. Chen, J. Wu, and M. Cardei, "A survey of attacks and countermeasures in mobile ad hoc networks," in Proc. Wireless Netw. Secur., 2007, pp. 103–135

Security is an essential service for wired and wireless network communications. The success of mobile ad hoc network (MANET) will depend on people 's confidence in its security. However, the characteristics of MANET pose both challenges and opportunities in achieving security goals, such as confidentiality, authentication, integrity, availability, access control, and non-repudiation. We provide a survey of attacks and countermeasures in MANET in this chapter. The countermeasures are features or functions that reduce or eliminate security vulnerabilities and attacks. First, we give an overview of attacks according to the protocol layers, and to security attributes and mechanisms. Then we present preventive approaches following the order of the layered protocol layers. We

also put forward an overview of MANET intrusion detection systems (IDS), which are reactive approaches to thwart attacks and used as a second line of defense

6. J. Sepúlveda, D. Flórez, M. Soeken, J. Diguet, and G. Gogniat, "Dynamic NoC buffer allocation for MPSoC timing side channel attack Protection," in Proc. IEEE 7th Latin Amer. Symp. Circuits Syst., Feb./Mar. 2016, pp. 91–94.

With the advances of chip manufacturing technologies, computer architects have been able to integrate an increasing number of processors and other heterogeneous components on the same chip. Network-on-Chip (NoC) is widely employed by multicore System-on-Chip (SoC) architectures to cater to their communication requirements. NoC has received significant attention from both attackers and defenders. The increased usage of NoC and its distributed nature across the chip has made it a focal point of potential security attacks. Due to its prime location in the SoC coupled with connectivity with various components, NoC can be effectively utilized to implement security countermeasures to protect the SoC from potential attacks. There is a wide variety of existing literature on NoC security attacks and countermeasures. In this article, we provide a comprehensive survey of security vulnerabilities in NoC-based SoC architectures and discuss relevant countermeasures.

3.METHODOLOGY

In figure, we can se the basic block diagram for the undersatanding of the project.

Block Diagram

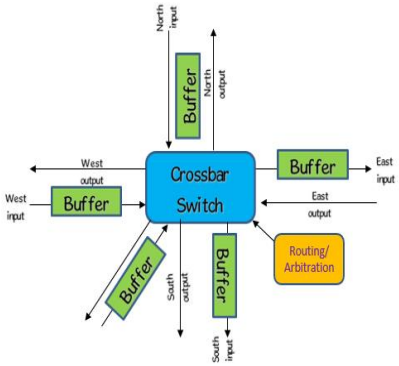

Figure 3.1

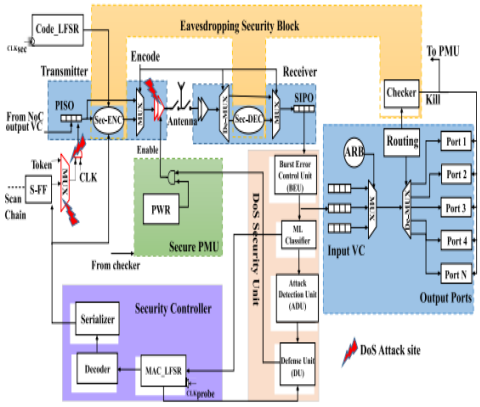

Figure 3.2 Wi NOC architecture

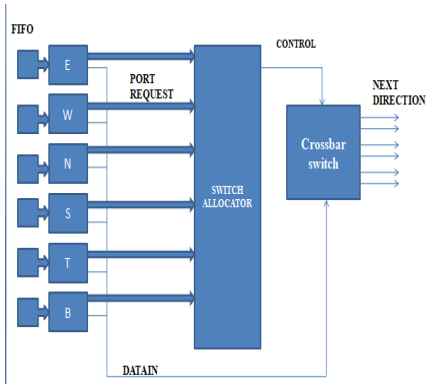

Figure 3.3 Proposed high performance routing model

3.1 FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-

programmable".The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard.The area of field programmable gate array (FPGA) design is evolving at a rapid pace. The increase in the complexity of the FPGA's architecture means that it can now be used in far more applications than before. The newer FPGAs are steering away from the plain vanilla type "logic only" architecture to one with embedded dedicated blocks for specialized applications.

Definitions of Relevant Terminology are Field-programmable Device (FPD) — a general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize difference PLA — a Programmable Logic Array (PLA) is a relatively small FPD that contains two levels of logic, an AND-plane and an OR-plane, where both levels are programmable. PAL— a Programmable Array Logic (PAL) is a relatively small FPD that has a programmable AND-plane followed by a fixed OR-plane. SPLD — refers to any type of Simple PLD, usually either a PLA or PAL. CPLD — a more Complex PLD that consists of an arrangement of multiple SPLD-like blocks on a single chip.

The FPGA Landscape

In the semiconductor industry, the programmable logic segment is the best indicator of the progress of technology. No other segment has such varied offerings as field programmable gate arrays. It is no wonder that FPGAs were among the first semiconductor products to move to the 0.13µm technology, and again recently to 90nm technology.

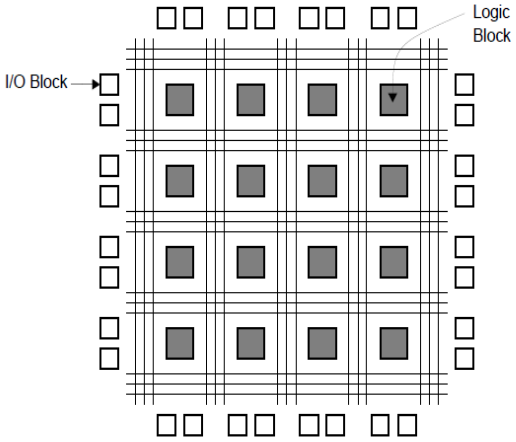

Figure 3.4 Structure of an FPGA

The players in the current programmable logic market are Altera, Atmel, Actel, Cypress, Lattice, Quick logic and Xilinx. Some of the larger and more popular device families are:Stratix™ from Altera, Accelerator from Actel, is XPGA™ from Lattice and Virtex™ fromXilinx Between these FPGA devices, many major electronics applications such as communications, video, image and digital signal processing, storage area networks and aerospace are covered.

4. HARDWARE AND SOFTWARE USED

BASIC HARDWARE COM PONENTS:

All networks are made up of basic hardware building blocks to interconnect network nodes, such as Network Interface Cards (NICs), Bridges, Hubs, Switches, and Routers. In addition, some method of connecting these building blocks is required, usually in the form of galvanic cable (most commonly Category 5 cable). Less common are microwave links (as in IEEE 802.12) or optical cable ("optical fiber").

Network Interface Cards

A network card, network adapter, or NIC (network interface card) is a piece of computer hardware designed to allow computers to communicate over a computer network. It provides physical access to a networking medium and often provides a low-level addressing system through the use of MAC addresses. Each network interface card has its unique id. This is written on a chip which is mounted on the card.

Repeaters

A repeater is an electronic device that receives a signal, cleans it of unnecessary noise, regenerates it, and retransmits it at a higher power level, or to the other side of an obstruction, so that the signal can cover longer distances without degradation. In most twisted pair Ethernet configurations, repeaters are required for cable that runs longer than 100 meters. A repeater with multiple ports is known as a hub. Repeaters work on the Physical Layer of the OSI model. Repeaters require a small amount of time to regenerate the signal. This can cause a propagation delay which can affect network communication when there are several repeaters in a row. Many network architectures limit the number of repeaters that can be used in a row (e.g. Ethernet's 5-4-3 rule).

Bridges

A network bridge connects multiple network segments at the data link layer (layer 2) of the OSI model. Bridges broadcast to all ports except the port on which the broadcast was received. However, bridges do not promiscuously copy traffic to all ports, as hubs do, but learn which MAC addresses are reachable through specific ports. Once the bridge associates a port and an address, it will send traffic for that address to that port only.

Bridges learn the association of ports and addresses by examining the source address of frames that it sees on various ports. Once a frame arrives through a port, its source address is stored and the bridge assumes that MAC address is associated with that port. The first time that a previously unknown destination address is seen, the bridge will forward the frame to all ports other than the one on which the frame arrived.

Switches

A network is a device that forwards and filters OSI layer 2 data grams (chunks of data communication) between ports (connected cables) based on the MAC addresses in the packets. [9] A switch is distinct from a hub in that it only forwards the frames to the ports involved in the communication rather than all ports connected. A switch breaks the collision domain but represents itself as a broadcast domain. Switches make forwarding decisions of frames on the basis of MAC addresses. A switch normally has numerous ports, facilitating a star topology for devices, and cascading additional switches. [10] Some switches are capable of routing based on Layer 3 addressing or additional logical levels; these are called multi-layer switches. The term *switch* is used loosely in marketing to encompass devices including routers and bridges, as well as devices that may distribute traffic on load or by application content (e.g., a Web URL identifier).

Routers

A router is an internetworking device that forwards packets between networks by processing information found in the datagram or packet (Internet protocol information from Layer 3 of the OSI Model). In many situations, this information is processed in conjunction with the routing table (also known as forwarding table). Routers use routing tables to determine what interface to forward packets (this can include the "null" also known as the "black hole" interface because data can go into it, however, no further processing is done for said data).

Firewalls

Firewalls are the most important aspect of a network with respect to security. A

firewalled system does not need every interaction or data transfer monitored by a human, as automated processes can be set up to assist in rejecting access requests from unsafe sources, and allowing actions from recognized ones. The vital role firewalls play in network security grows in parallel with the constant increase in 'cyber' attacks for the purpose of stealing/corrupting data, planting viruses, etc.

Cyclone IIII 3C16 FPGA

- 15,408 Les.
- 56 M9K Embedded Memory Blocks.
- 504K total RAM bits.
- 56 embedded multipliers.
- 4 PLLs.
- 346 user I/O pins.

Built-in USB Blaster circuit

- On-board USB Blaster for programming and user API (Application programming interface) control.
- Using the Altera EPM240 CPLD.

SDRAM

- One 8-Mbyte Single Data Rate Synchronous Dynamic RAM memory chip.
- Supports 16-bits data bus.

Flash memory

- 4-Mbyte NOR Flash memory.
- Support Byte (8-bits)/Word (16-bits) mode.

SD card socket

- Provides both SPI and SD 1-bit mod SD Card access.

Push button switches

pushbutton switches , Normally high; generates one active-low pulse when the switch is pressed.

Slide switches

- 10 Slide switches.
- A switch causes logic 0 when in the DOWN position and logic 1 when in the UP position.

General User Interfaces

- 10 Green color LEDs (Active high).
- 4 seven-segment displays (Active low).
- 16x2 LCD Interface (Not include LCD module).

Clock inputs

- 50-MHz oscillator.

VGA output

- Uses a 4-bit resistor-network DAC.
- With 15-pin high-density D-sub connector.
- Supports up to 1280x1024 at 60-Hz refresh rate.

Serial ports

- One RS-232 port (Without DB-9 serial connector).
- One PS/2 port (Can be used through a PS/2 Y Cable to allow you to connect a keyboard and mouse to one port).

Two 40-pin expansion headers

- 72 Cyclone III I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives.

4.1 SOFTWARES USED

We have used Modelsim, and QuartersII. Let us see in brief

MODEL SIM :

High Performance and Capacity Mixed HDL Simulation – Model Sim Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and SystemC. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA design.

The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

ModelSim-Altera Edition

- Recommended for simulating all FPGA designs (Cyclone®, Arria®, and Stratix® series FPGA designs).
- 33 percent faster simulation performance than ModelSim®-Altera® Starter Edition.
- No line limitations.

QUARTUS II:

Quartus II is a software tool produced by Altera for analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Quartus II Web Edition

The Web Edition is a free version of Quartus II that can be downloaded or delivered by mail for free. This edition provided compilation and programming for a limited number of Altera devices.

The low-cost Cyclone family of FPGAs is fully supported by this edition, as well as the MAX family of CPLDs, meaning small developers and educational institutions have no overheads from the cost of development software .License registration is required to use the Web Edition of Quartus II, which is free and can be renewed an unlimited number of times.

Quartus II Subscription Edition

Quartus II Subscription Edition is also available for free download, but a license must be paid for to use the full functionality in the software. The free Web Edition license can be used on this software, restricting the devices that can be used.

5.RESULT AND DISCUSSION

SIMULATION OUTPUT

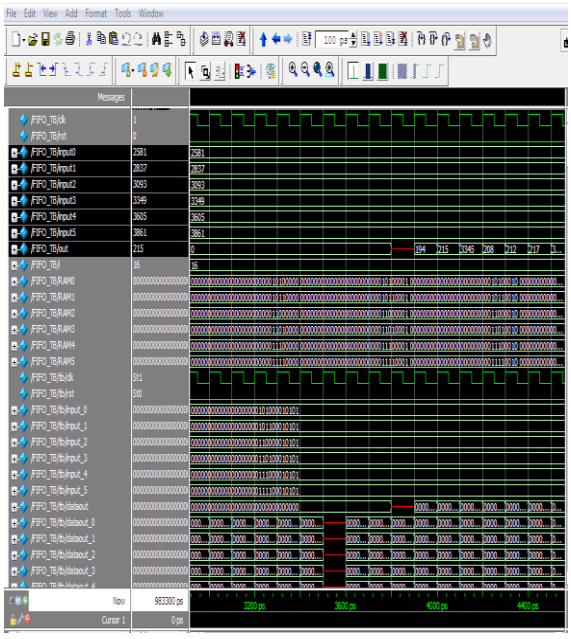

Figure 5.1 Modelsim simulated output

AREA UTILIZATION REPORT

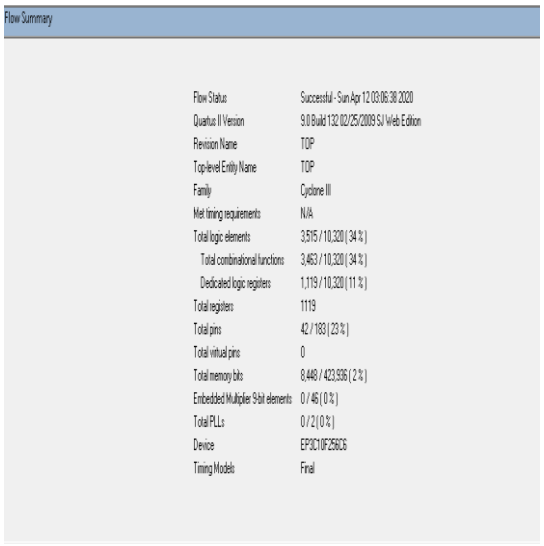

Figure 5.2 Flow summary report

P

ERFORMANCE REPORT:

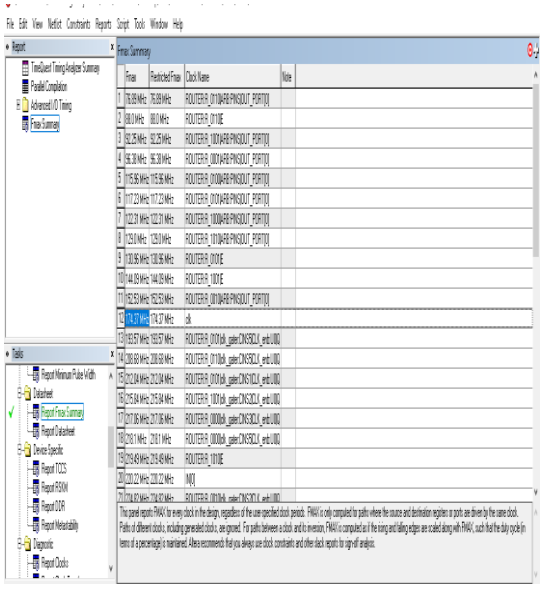

Figure 5.3 Fmax. summary report

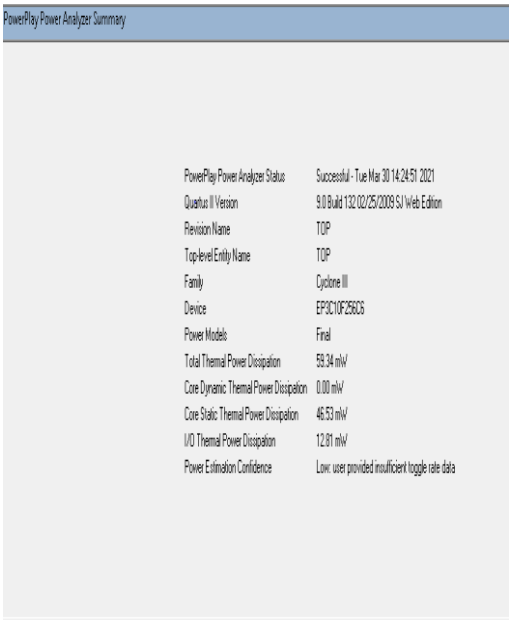

Figure 5.7 Power dissipation report

SYNTHESIS REPOR

TABLE I

Trade off analyzes of pipelining NoC with bypass data forwarding using QUARTUS II hardware synthesis in CYCLONE III family

POWERANALYSES

WiNOC model	AREA (LEs)	Fmax (SPEED)
Without pipelining	3248	136.69 MHz
Pipelining bypass enabled router model	3515	174.37 MHz

6.CONCLUSION

NoC is the solution for intercommunication of SoC such as parallel communication wires and also removes barriers to bus-based communication. In this paper, an advanced memory unit is proposed and implemented in Bi-NoC to achieve less memory. A buffer is needed as well as high performance in terms of maximum operating bandwidth. Pared to previous work, the proposed work improved approximately 28% delay and 17% resources utilization. As RingNet[15] used Round robin arbiter, the resources utilization is more than proposed work. The data packets are divided into flits and the buffered data is shared between neighbour routers, resulting in a smaller buffer size when data is transferred over data flits. Router configuration integrated into the Bi-NoC configuration for higher data transfer speeds than a typical NoC. It is virtualized.

As a result of creating channels between routers when data flow is blocked, the latency of data packets is reduced as well as dead lock errors are avoided. ults are improved in terms of resource utilization when compared with existing work. In future, NoC based processors are used at Artificial Intelligence applications. The performance of the NoC must be improved by advancing router components since power consumption increased through virtual channels at an advanced FIFO structure.

7.REFERANCES

[1] U. Y. Ogras and R. Marculescu, "'It's a small world after all': NoC performance optimization via long-range link insertion," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 7, pp. 693–706, Jul. 2006.

[2] L. P. Carloni, P. Pande, and Y. Xie, "Networks-on-chip in emerging interconnect paradigms: Advantages and challenges," in Proc. ACM/IEEE Int. Symp. Netw.-on-Chip, May 2009, pp. 93–102.

[3] M. P. D. Sai, H. Yu, Y. Shang, C. S. Tan, and S. K. Lim, "Reliable 3-D clock-tree synthesis considering nonlinear capacitive TSV model with electrical–thermal–mechanical coupling," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 11, pp. 1734–1747, Nov. 2013.

[4] A. Ganguly et al., "Intra-chip wireless interconnect: The road ahead," in Proc. Int. Workshop Netw. Chip Architectures, Oct. 2017, p. 3.

[5] B. Wu, J. Chen, J. Wu, and M. Cardei, "A survey of attacks and countermeasures in mobile ad hoc networks," in Proc. Wireless Netw. Secur., 2007, pp. 103–135.

[6] J. Sepúlveda, D. Flórez, M. Soeken, J. Diguet, and G. Gogniat, "Dynamic NoC buffer allocation for MPSoC timing side channel attack Protection," in Proc. IEEE 7th Latin Amer. Symp. Circuits Syst., Feb./Mar. 2016, pp. 91–94.

[7] S. Manoj P. D. et al., "A scalable network-on-chip microprocessor with 2.5D integrated memory and accelerator," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 6, pp. 1432–1443, Jun. 2017.

[8] P. Cotret, J. Crenne, G. Gogniat, J. Diguet, L. Gaspar, and G. Duc, "Distributed security for communications and memories in a multiprocessor architecture," in Proc. IEEE Int. Symp. Parallel Distrib. Process. Workshops Phd Forum, May 2011, pp. 326–329.

[9] C. H. Gebotys and R. J. Gebotys, "A framework for security on NoC technologies," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI, Feb. 2003, pp. 113–117.

[10] A. Ganguly, M. Y. Ahmed, and A. Vidapalapati, "A denial-of-service resilient wireless NoC architecture," in Proc. Great Lakes Symp. VLSI, May 2012, pp. 259–262.